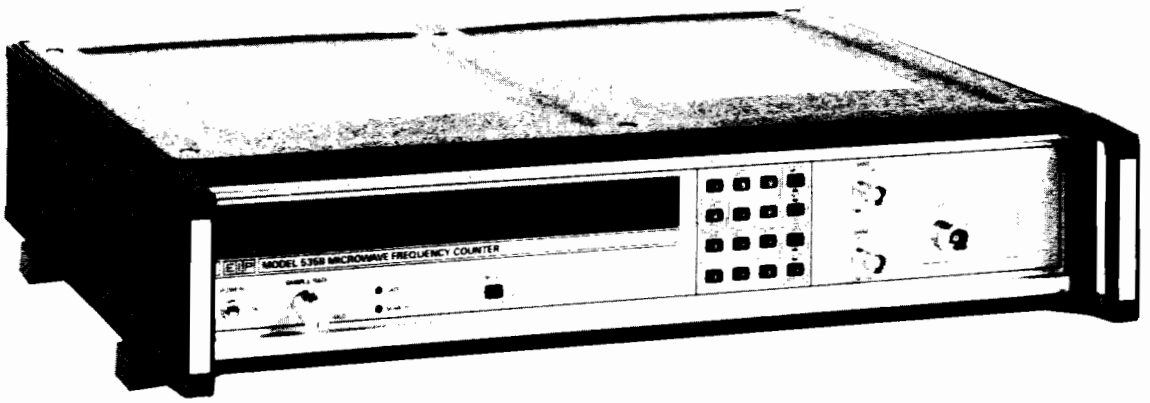

Models 535B & 538B
Microwave Frequency Counters

EIP Microwave, Inc.
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New editions incorporate all update material since the previous edition. The date on the title page changes only when a new edition is published. If minor corrections and updates are incorporated, the manual is reprinted but the date and edition number on the title page do not change.

FIRST EDITION ..... *February 1988*

Certification

EIP Microwave certifies that this instrument was thoroughly inspected and tested, and found to be in conformance with the specifications noted herein at time of shipment from factory.

Warranty

EIP Microwave warrants this counter to be free from defects in material and workmanship for one year from the date of delivery. Damage due to accident, abuse, or improper signal level, is not covered by the warranty. Removal, defacement, or alteration, of any serial or inspection label, marking, or seal, may void the warranty. EIP Microwave will repair or replace at its option, any components of this counter which prove to be defective during the warranty period, provided the entire counter is returned PREPAID to EIP or an authorized service facility. In-warranty counters will be returned freight prepaid; out-of-warranty units will be returned freight COLLECT. No other warranty other than the above warranty is expressed or implied.

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Section 1
General Information

DESCRIPTION

The 535B/538B series counters are microprocessor-based heterodyne instruments. The 535 and 538 span the frequency range from 10 Hz to 20 GHz and 10 Hz to 26.5 GHz respectively.

Through keyboard control, the 53XB series counters provide frequency offsets and frequency multiplication. Options include full systems capability via GPIB, high stability time bases, and frequency extension to 20 GHz for 535B. Measurements are presented on a 12 digit LED display that is sectionalized to read GHz, MHz, kHz, and Hz.

Full frequency range is covered in three bands. Band 1 is a high impedance input (1 M ohm/20 pF) and spans a 10 Hz to 100 MHz range, with a sensitivity of 25 mV RMS. Band 2 has an input impedance of 50 ohms, a 10 MHz to 1 GHz range, a sensitivity of -20 dBm. Band 3 has an input impedance of 50 ohm nominal over a range of 1 GHz to 20 GHz (or 26.5 GHz), and a sensitivity to -30 dBm (typical).

SPECIFICATIONS, continued

BAND 1	
RANGE	10 Hz to 100 MHz
SENSITIVITY	25 mV rms
IMPEDANCE	1 M ohm/20 pF
CONNECTOR	BNC (female)
MAX. INPUT LEVEL	120 V rms *
DAMAGE LEVEL	150 V rms *
	* (Above 1 kHz max. input will decrease at 6 dB/octave down to 3.0 V rms.)

BAND 2	
RANGE	10 MHz to 1 GHz
SENSITIVITY	-15 dBm with Option 12: -20 dBm
DYNAMIC RANGE	30 dB
IMPEDANCE	50 ohms Nominal
CONNECTOR	BNC (female)
MAX. INPUT LEVEL	+10 dBm
DAMAGE LEVEL	+27 dBm
ACQUISITION TIME	<50 msec

BAND 3 RANGE	Model 535B: 1 GHz to 20 GHz Model 538B: 1 GHz to 26.5 GHz
SENSITIVITY (0° to 50° C)	1 GHz to 12.4 GHz: -25 dBm with Option 12: -30 dBm 12.4 GHz to 20 GHz: -20 dBm with Option 12: -25 dBm 20 GHz to 26.5 GHz: -15 dBm with Option 12: -20 dBm
DYNAMIC RANGE (Typical)	1 GHz to 12.4 GHz, 35 dB 20 GHz to 26.5 GHz, 25 dB 12.4 GHz to 20 GHz, 30 dB
IMPEDANCE	50 ohms Nominal
CONNECTOR	Model 535B: Precision Type N (female) Model 538B: APC - 3.5 (female)
MAX. INPUT LEVEL	+10 dBm
DAMAGE LEVEL	10 Watts, (+40 dBm)
ACQUISITION TIME	< 200 msec Independent of frequency
AUTO AMPLITUDE DISCRIMINATION	(Automatic amplitude discrimination of two frequencies) 10 dB
FM MODULATION	20 MHz p-p up to 10 MHz rate
VSWR	< 2.5: 1 typical

TIME BASE FREQUENCY	10 MHz TCXO
AGING RATE	$<\|1 \times 10^{-7}\|$ per month, 1×10^{-6} |per year after 30 days
SHORT TERM	$<\|1 \times 10^{-9}\|$rms for one second averaging time
TEMPERATURE	$<\|1 \times 10^{-6}\|$ 0° to 50° C when set at 25° C
LINE VARIATION	$<\|1 \times 10^{-7}\| \pm$ 10% change.
WARM UP TIME	NONE
OUTPUT FREQUENCY	10 MHz, square-wave, 1 V p-p minimum into 50 ohms.
EXT. TIME BASE	Requires 10 MHz, 1 V p-p minimum into 300 ohms
PHASE NOISE	-95 dBc/Hz at 10 Hz from carrier

SPECIFICATIONS

GENERAL	
RESOLUTION	Front panel keyboard input select 0.1 Hz to 1 GHz 0.1 Hz resolution Band 1 only. No frequency offset or multiplier in 0.1 Hz resolution.
MEASUREMENT TIME	1 msec for 1 kHz resolution 1 sec for 1 Hz resolution
DISPLAY	12 digit LED sectionalized
ACCURACY	± 1 count ± time base errors
TEST	Front panel selected diagnostics
SAMPLE RATE	Controls time between measurements variable from 100 msec typ. to 10 sec. Switchable Hold position holds display indefinitely.
RESET	Resets display to zero and initiates new reading
OFFSETS	Keyboard control of frequency offsets. Displayed frequency is offset by entering value to 1 Hz resolution.
MULTIPLY	Keyboard control of frequency multiply. Display frequency is multiplied by 1-99.
OPERATION TEMP.	0° C to 50° C
POWER	100/120/220/240/VAC ± 10% (selectable) 50 to 60 Hz. 60 VA typical
WEIGHT, NET	~ 26 lb (11.8 kg)
WEIGHT, SHIPPING	~ 32 lb (14.5 kg)
DIMENSIONS (HWD)	3.5'' x 16.75'' x 14.0'' (89 mm x 425 mm x 356 mm)
ACCESSORIES FURNISHED	Power Cord and Manual

BAND 4 Used with 538B/06 Counter and 590 Frequency Extension Kit	
OPTION	91
SELECT BAND	41
Waveguide Band	Ka
Range	26.5-40 GHz
Sensitivity (typ)	-25dBm (-20 dBm min)
Waveguide Size	WR-28
Waveguide Flange	UG-599/U
Max. Input (typ)	+5 dBm
Damage Level	+10 dBm
Aquisition Time (typ)	<1 sec

TIME BASE OSCILLATOR OPTIONS: (See Section 10 for detailed information

	03	04	05
AGING RATE/24 HOURS (After 72 hour warm-up)	$< \mid 5 \times 10^{-9} \mid$	$< \mid 1 \times 10^{-9} \mid$	$< \mid 5 \times 10^{-10} \mid$
SHORT TERM STABILITY (1 second average)	$< \mid 1 \times 10^{-10}$ rms	$< \mid 1 \times 10^{-10}$ rms	$< \mid 1 \times 10^{-10}$ rms
0° to +50° C TEMPERATURE STABILITY	$< \mid 6 \times 10^{-8} \mid$	$< \mid 3 \times 10^{-8} \mid$	$< \mid 3 \times 10^{-8} \mid$
± 10% LINE VOLTAGE CHANGE	$< \mid 5 \times 10^{-10} \mid$	$< \mid 2 \times 10^{-10} \mid$	$< \mid 2 \times 10^{-10} \mid$
08 GPIB - Provides sprogramming and output capability per IEEE 488-1978.			
09 REAR INPUT			
10 CHASSIS SLIDES			
12 +5 dB SENSITIVITY			

Section 2
Installation

INSTALLATION

No special installation instructions are required. The counter is a self-contained bench or rack mounted unit, and only requires connection to a standard 100/120/220/240V 50-60 Hz power line for operation.

CAUTION

Check current rating of counter fuse and setting of rear panel VAC selector switch before applying power to counter.

COUNTER IDENTIFICATION

This counter is identified by two sets of numbers, the model number 535B or 538B and a serial number that is located on a label affixed to the rear panel. Both numbers must be mentioned in any correspondence regarding this counter.

SHIPPING AND STORAGE

Wrap the counter in heavy plastic or kraft paper and repack in original container if available. If the original container cannot be used, use a heavy (275-pound test) double-walled carton with approximately four inches of packing material between the counter and the inner carton. Seal the carton with strong filament tape or strapping. Mark the carton to indicate that it contains a fragile electronic instrument. Ship to the EIP address on the title page of this manual.

PERFORMANCE CHECKOUT PROCEDURE

The following procedure can be performed without special tools or equipment.

1. Turn counter power switch off. Check fuse rating and setting of AC POWER switch on rear panel.
2. Connect power cord to 100/120 or 220/240 V, 50-60 Hz single-phase power source. The ground terminal on the power cord plug should be grounded.
3. Turn POWER switch on. Dashes will be displayed for about one second, followed by all 0's. This indicates that automatic self-check has been completed.
4. Press TEST [0] [1]. Display should read 200 000 000 ±1.
5. Press TEST [0] [2]. Display should read all 8's and all annunciators should be lit.
6. Press TEST [0] [3]. Each display segment should light in turn.
7. Press TEST [0] [4]. Each digit should light in turn.
8. This completes the performance checkout procedure.

Section 3
Operation

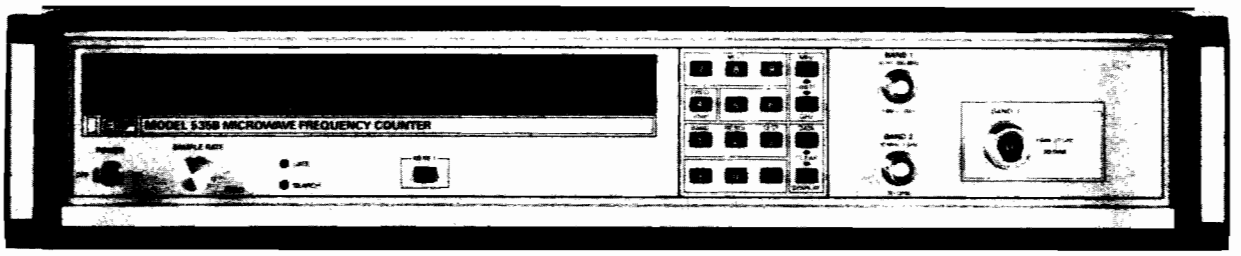


Figure 3-1. Front Panel, Model 535B

FRONT PANEL CONTROLS AND INDICATORS

DISPLAY

- The 12 digit LED display provides a direct numerical readout of a measurement or of an input frequency. The frequency readout is displayed in a fixed position format that is sectionalized in GHz, MHz, kHz and Hz.
- POWER switch turns counter on.
- SAMPLE RATE/HOLD varies time between measurements from 0.1 to 10 seconds (nominal). (Gate time is added to sample time, thus the minimum reading for 1 Hz resolution is 1.1 seconds.) The last reading is retained indefinitely in HOLD.
- GATE lights when the signal gate is open and a measurement is being made.
- SEARCH lights when the counter is not locked to an input signal.
- RESET manually over-rides all controls, resets the counter and converter, and initiates a new reading.

OPERATING STATUS

The operating status of the counter is indicated by a series of LEDs. When the counter is displaying input data, instead of a measurement, the appropriate LED status indicator will flash.

- REMOTE lights to indicate that front panel controls are disabled, and that the counter is being controlled by the GPIB option (08)
- EXT REF lights to indicate the counter is set to an external time base reference.

CAUTION

When EXT REF lights it does NOT indicate that correct signal level has been applied.

- OFFSET, FRQ lights when frequency offsets are stored in the counter memory.
- Band 1, 2, 3 light to indicate which operating range has been selected.
- MLT lights to indicate the multiplier function is active.

SIGNAL INPUT

- Band 1 input connector (BNC female) has a nominal input impedance of 1 Meg ohms, shunted by 20 pF. It is used for measurements in the range of 10 Hz to 100 MHz.
- Band 2 input connector (BNC female) has a nominal input impedance of 50 ohms. It is used for measurements in the range of 10 MHz to 1 GHz.
- Band 3 input connector on the 535 is a precision type N female. It is used for counter operation in the range of 1 GHz to 18 GHz (20 GHz with Option 11). Model 538 has an APC-3.5 female connector that is used for operation in the range of 1 GHz to 26.5 GHz.

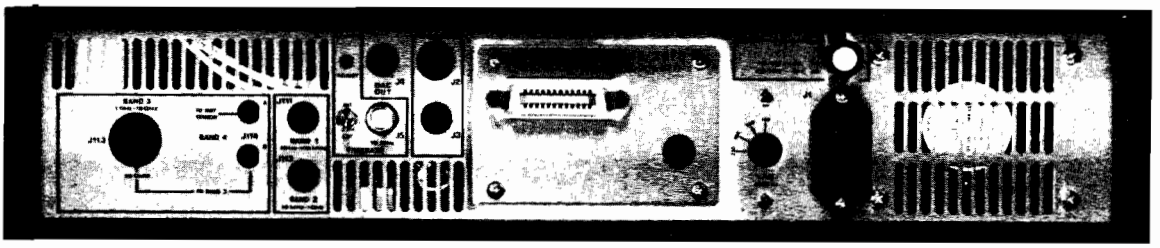


Figure 3-3. Rear Panel

REAR PANEL CONTROLS AND CONNECTORS

- TIME BASE ADJUST control is used with options 03, 04, or 05 only. Screwdriver adjustment allows precise setting of the internal ovenized crystal oscillator.
- TIME BASE INT/EXT switch selects either the internal time base or an external 10 MHz reference.
- TIME BASE connector (BNC female) allows monitoring of internal 10 MHz time base, or input of an external 10 MHz reference.
- GPIB connector is used with the IEEE 488 - 1978 General Purpose Interface Bus option (08).
- FUSE provides overload protection. Use a 1 amp slow-blow MDL type fuse for 100/120 V operation. Use a .50 amp slow-blow FST type fuse for 220/240 V operation.
- VAC SWITCH sets the operating voltage of the counter to match power line. There are 4 settings: 100, 120, 220, and 240 VAC. Counter will operate at voltages within ±10% of selected line voltage, at frequencies of 50 to 60 Hz.
- AC POWER connector accepts the power cord supplied with the counter.

CAUTION

Switch setting and fuse rating must match power line voltage.

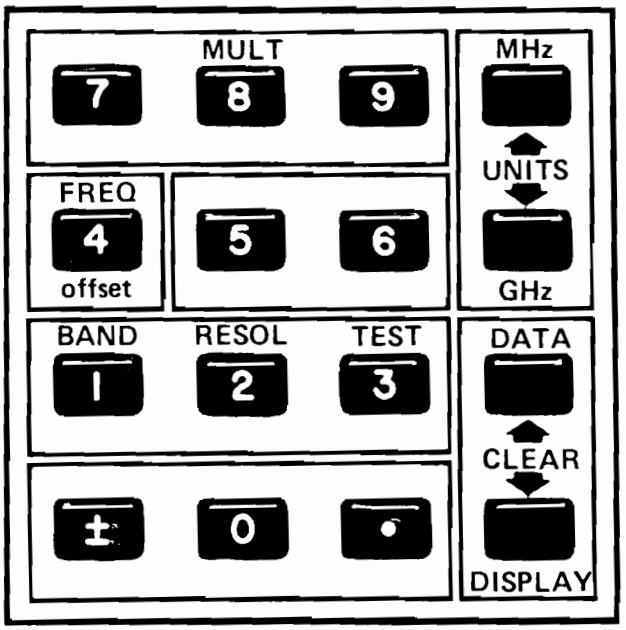


Figure 3-4. Keyboard

KEYBOARD

The keyboard consists of 16 pushbuttons that control major functions of the counter. Twelve keys are used for numerical data entry, the digits 0 through 9, the decimal point and the minus sign. Two keys (MHz and GHz) act as terminators for the input of frequency offset or frequency limits. The CLEAR DATA and CLEAR DISPLAY keys are used to clear stored or displayed data. Five of the numerical keys are also used to select the band, resolution, test function, frequency offset, and multiplier function.

UNITS (MHz/GHz)

PRESS: MHz Completes Entry Sequence

PRESS: GHz Completes Entry Sequence

CLEAR (DATA/DISPLAY)

PRESS: DATA CLEAR Return "STORED" data of selected function to Power On state. Clears Limits (Low/High), Offsets, DAC, and multiplier operations.

PRESS: CLEAR DISPLAY Clears display. Does not affect stored data. Restores counter to measurement mode.

BAND SELECTION

To select one of three standard operating bands on the model 535B or 538B.

PRESS: BAND 1 or PRESS: BAND 2 or PRESS: BAND 3

Notice annunciator flash and selected band number will light when chosen. This feature allows multiple inputs to be connected and selected in turn.

The "BAND" KEY followed by a numeric key enables the following band selection.

PRESS: BAND 1	10 Hz - 100 MHz Input
PRESS: BAND 2	10 MHz - 1 GHz Input
PRESS: BAND 3	1 GHz - 20 GHz (Model 535B) 26.5 GHz (Model 538B)

RESOLUTION/GATE TIME SELECTION

The "RESOL" key followed by a numeric key enables following resolutions.

PRESS: RESOL 0 — 1 Hz RESOLUTION

PRESS: RESOL 1 — 10 Hz RESOLUTION

PRESS: RESOL 2 — 100 Hz RESOLUTION

PRESS: RESOL 3 — 1 KHz RESOLUTION

PRESS: RESOL 4 — 10 KHz RESOLUTION

PRESS: RESOL 5 — 100 KHz RESOLUTION

PRESS: RESOL 6 — 1 MHz RESOLUTION

PRESS: RESOL 7 — 10 MHz RESOLUTION

PRESS: RESOL 8 — 100 MHz RESOLUTION

PRESS: RESOL 9 — 1 GHz RESOLUTION

0.1 HZ RESOLUTION

The user can select 0.1 Hz resolution in Band 1. In order to extend the resolution to 0.1 Hz, the gate time inside the counter is increased to 10 seconds. Therefore, if the count chain reads 11 after the 10-second gate period, then the frequency displayed is 1.1 Hz.

The significance of the digits on the front panel is shifted left three digits. If the frequency of the input signal is 9 MHz, the counter displays 9 GHz.

If the user changes the resolution during the 10-second gate period, the counter still has to wait for the 10-second gate to complete before it changes the gate time accordingly.

To change the counter gate time to 10-seconds through front panel:

1. Select "band 1".
2. Enter "res", ".1".

To change the counter gate time to 10-seconds via GPIB:

1. Command the counter "B1R.1"

To change the counter gate time to 10-seconds via MATE (Option 13), enter the following commands:

1. "CLS :CH01"
2. "FNC ACS FREQ :CH01 SET FRES 0.1".

As the resolution is decreased from 1 Hz to 1 kHz, the gate time LED should cycle faster:

- 1 Hz resolution equals a gate time of 1 sec.
- 10 Hz = 100 msec Gate time
- 100 Hz = 10 msec Gate time
- 1 kHz to 1 GHz = 1 msec Gate time

DISPLAY AND DATA ENTRY SEQUENCE

The keyboard display and data entry sequences are segmented into four main groups. All keyboard operations must be started by choosing the function first.

DATA ENTRY - enters offsets

Sequence:
1. FUNCTION, SIGN (plus sign not required), NUMBER, DECIMAL, NUMBER, UNITS (decimal and second number is optional).
2. FUNCTION, NUMBER

Examples:
1. FREQ OFFSET [±] [1] [•] [2] GHz
2. BAND [2]

DISPLAY DATA - display previously entered data

Sequence: FUNCTION, CLEAR DISPLAY

Example: FREQ OFFSET, CLEAR DISPLAY

CLEAR DATA - clear entered data

Sequence:
1. FUNCTION, CLEAR DATA
2. FUNCTION , [0] , UNITS
3. FUNCTION , UNITS

Examples:
1. FREQ OFFSET, DATA CLEAR
2. FREQ OFFSET [0] GHz
3. FREQ OFFSET GHz

CLEAR ENTRY - clear display before completing data entry

Sequence: FUNCTION , STRING , CLEAR DISPLAY

Example: FREQ OFFSET [1] [•] [2] CLEAR DISPLAY

MULTIPLY FUNCTION:

In the multiply function the measured frequency is multiplied by an integer up to 99. The result is displayed to 1 KHz resolution. If the results of the multiplications are too big for the front panel to display, the front panel will show F's.

EXAMPLES: PRESS [MULT] AND KEY IN TWO DIGIT NUMBER

EXAMPLE [MULT] [0] [2] FOR MULTIPLIER = 2

NOTE: When "MULT" key is pressed the annunciator "MLT" will flash until the sequence is completed. The two digit multiplier (m) will be displayed as the numbers are entered.

To clear the multiplier function the following operation is performed.

PRESS [MULT] [CLEAR DATA] or PRESS [MULT] [0] [1]

This sequence clears the multiplier function and multiplier (m).

mX ± b

By using the frequency offsets and multiply functions the counter can automatically perform mX ± b calculations.

The equation for the function performed is:

Displayed Reading = mX ± b where m = Multiplier (up to 99) entered from keyboard.

X = Input frequency.

± b = Frequency offset entered from the keyboard.

TO DO mX ± b CALCULATION FOR m = 2, b = -70 MHz

PRESS [MULT] [0] [2] AND [FREQ OFFSET] [±] [7] [0] [MHz]

TEST SELECTION

The following tests will verify proper operation of most functional areas of the counter. At the initial turn on the counter performs a RAM and PROM check. During this check dashes are displayed until the check has been completed.

RAM and PROM

The processor writes a sequential bit pattern to each RAM location, then independently reads that pattern. Thus each bit in each location is checked. If the RAM check fails the display will show all "E's". This indicates that the RAM or the RAM decoding is faulty.

The PROM check verifies the PROM bit pattern. If the PROM check fails an error message will be displayed. This indicates that the PROM's or the PROM decoding is faulty. See Section 6.

If both RAM and PROM check are good the counter will begin normal operation about one second after turn on. The counter will now display all 0's.

200 MHz SELF TEST

PRESS: TEST [0] [1]

Notice display is 200 MHz. This verifies operation of the time base reference and it's associated circuits, the signal selection, the count chain, and the local oscillator.

LED TEST

PRESS: TEST [0] [2]

Notice all LED segments and yellow annunciators are lit. This verifies operation of all visual indicators

LED SEGMENT TEST

PRESS: TEST [0] [3]

Notice each segment of each display digit is lit in turn. The sample rate pot will change the rate, and may be adjusted. This checks the segment drivers.

DISPLAY DIGIT TEST

PRESS: TEST [0] [4]

Notice all segments of each digit are lit in turn to verify that each digit operates independently.
The sample rate pot will change the rate, and may be adjusted.

KEYBOARD TEST

PRESS: TEST [ ] [0] [5]

Notice display is 05. Press any key and display will indicate a two digit number showing the position of that key within the matrix thus checking keyboard operations. See Figure 6-5 for coordinates.

TO EXIT TESTS

PRESS: CLEAR DISPLAY to exit a test and return to normal operation.

To exit tests 1 through 4, 6 and 7 you can press any function key. This will exit the test and enter the function selected.

FREQUENCY OFFSETS

Frequency OFFSETS can be added or subtracted from the measured value. These OFFSETS can be entered via the front panel keyboard to 1 Hz resolution:

PRESS: FREQ OFFSET Notice the flashing annunciator.

PRESS: Number keys corresponding to desired frequency OFFSETS. If OFFSET is to be subtracted press [±] and notice polarity sign indicator at far left of display.

PRESS: MHz or GHz to integrate programmed OFFSET into actual frequency measurement. Notice solidly lit annunciator indicating instrument memory is loaded.

PRESS: FREQ OFFSET Recalls OFFSET to display, FRQ and OFFSET annunciators flashing.

PRESS: CLEAR DISPLAY Notice frequency displayed includes OFFSET; annunciators are lit continuously.

PRESS: FREQ OFFSET Recalls OFFSET to display, FRQ and OFFSET annunciators flashing.

PRESS: CLEAR DATA Clears data memory and clears offset. FRQ and OFFSET annunciators are out. Display is actual frequency without offset.

SET-UP FOR BASIC FREQUENCY MEASUREMENT

Choose the input band by pressing [BAND] and a number key corresponding to the band. Choose resolution by pressing [RESOL] and a number key corresponding to required resolution. The signal coupled to the selected input Band Connector will be automatically displayed to the resolution chosen.

NOTE: When pressing the RESOL key the display will go blank for approximately 1/4 second.

DISPLAY ERROR MESSAGES

When an error occurs the error number will be displayed. The probable cause of each error is listed below.

OPERATOR ERRORS

The following error messages indicate an operator error.

01 Illegal Key Sequence.

02 A resolution number was not entered.

03 A band number was not entered; or the number entered was too large.

04

05

06

07

08

09 Illegal test mode key sequence.

10

11 Illegal Multiplier key sequence.

12

13 Option not installed.

COUNTER ERRORS

The following error messages indicate a malfunction within the counter.

31	Check sum error	Section 1 PROM	D0000 - DFFF	A105, U13
32	Check sum error	Section 2 PROM	E000 - EFFF	A105, U17
33	Check sum error	Section 3 PROM	E000 - FFFF	A105, U15
36	Check sum error	GPIB PROM	C800 - CFFF	A105, U16

Section 4
Theory of Operation

GENERAL

The 535B and 538B counters automatically measure and display the frequency of an input signal within the range of 10 Hz to 20 GHz for the 535B, and 10 Hz to 26.5 GHz for the 538B. The frequency range is divided into three bands in both models.

BAND 1 operates from 10 Hz to 100 MHz. An impedance converter provides an input impedance of 1 M ohm, shunted by 20 pF.

BAND 2 operates from 10 MHz to 1 GHz, using a heterodyne down converter which converts the input signal into an output signal with a range of 10 MHz to 190 MHz.

BAND 3 operates in the microwave range of 1 to 20 GHz (or 26.5 GHz) and uses a YIG tuned heterodyne converter to translate the input frequency downward to an intermediate frequency (IF) of 127 MHz.

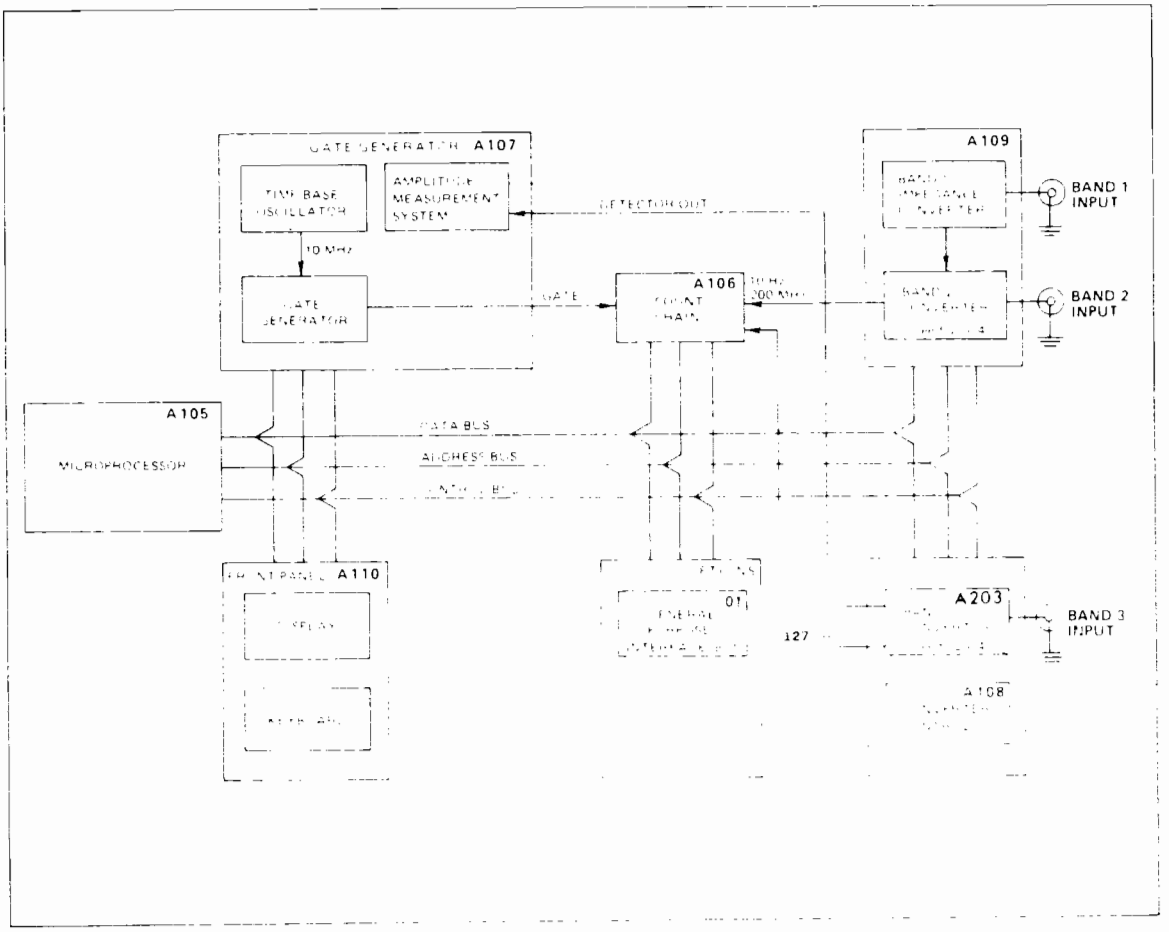


Figure 4-1. Counter Block Diagram, Simplified

BASIC COUNTER

Overall operation is controlled by the Microprocessor Assembly A105. This assembly contains an eight bit microprocessor, its control logic, and the system memory. It communicates with all other assemblies in the instrument by means of a triple bus system: the data, address, and control bus. On each assembly there is a Peripheral Interface Adaptor (PIA) which provides the interface between the bus system and the instrument hardware.

Frequency measurements are performed by comparing an unknown signal to a reference frequency, namely the time base. A 10 MHz crystal oscillator is used as the internal reference and is a part of the Gate Generator Assembly A107. For increased accuracy and stability, ovenized oscillator options are available, or the user may select an external 10 MHz reference.

A frequency measurement is made by generating a time interval (Gate Time) consisting of a number of cycles of the reference. This Gate Time is then used as an interval during which the input signal is counted by the Count Chain Assembly A106.

Initially, the microprocessor selects one of several available inputs to the Count Chain Assembly and the appropriate Gate Time based on user input information, band selection, resolution, etc. The microprocessor then initiates the measurement cycle by resetting the Count Chain to zero and allowing a gate to be generated. During the gate interval, the Count Chain accumulates the number of cycles of the input signal. At the end of the gate time, the microprocessor reads the stored information in the Count Chain and performs any required calculations necessary to convert the measurement into a direct reading of the unknown frequency. The front panel display is then updated with the new measurement results. Figure 4-1 shows a simplified block diagram of the counter.

BAND 2 CONVERTER

An input signal is applied to the mixer along with an appropriate local oscillator (L.O.) to generate an IF frequency in the range of 10 MHz to 190 MHz. This signal is filtered and amplified to a level suitable for direct measurement by the Count Chain.

The L.O. frequency is generated by the Voltage Controlled Oscillator (VCO) of the Band 3 Converter. This frequency is phase locked to the counter's time base and controlled by the microprocessor. A VCO multiplier serves to either pass along the signal directly or double it. It can also turn off the signal and pass only a DC bias to the mixer.

Two detectors provide outputs proportional to the amplitudes of both the applied RF signal and the resulting IF signal. These outputs are compared in the Signal Comparator, which provides a digital output when the IF amplitude exceeds the RF amplitude.

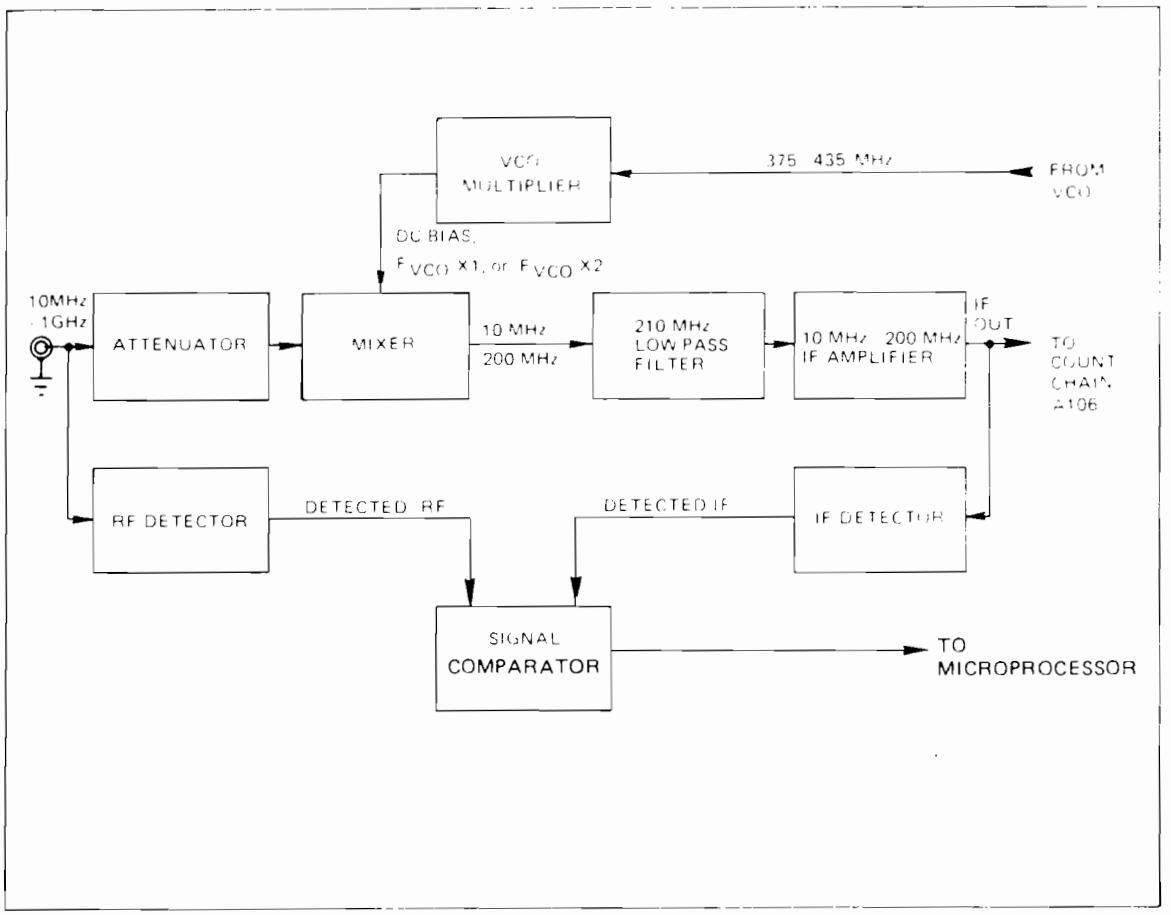


Figure 4-2. Band 2 Converter Block Diagram, Simplified

The output frequency of the system is the difference between the input signal and the L.O. applied to the mixer. Since the L.O. frequency is a harmonic (N) of the VCO frequency, the unknown input frequency can be expressed as $F_{IN}=N F_{VCO} \pm F_{IF}$. There are three primary functions of the software operating the converter:

- To select the appropriate harmonic number N.
- To select an appropriate VCO frequency.
- To determine whether the IF frequency is added to, or subtracted from the L.O. frequency.

These functions are accomplished by selecting N and F_{VCO} and looking for an IF signal of the appropriate amplitude and frequency. Overall system gain is such that whenever the correct L.O. frequency is applied, the IF power will exceed the RF power. This is the primary information used in determining the correct VCO frequency and harmonic number. Once an IF is obtained, the harmonic number is verified and the +/- sign in the equation is determined by shifting the VCO frequency and observing the magnitude and direction of the resulting IF shift. Converter operation is diagrammed in Figure 4-3.

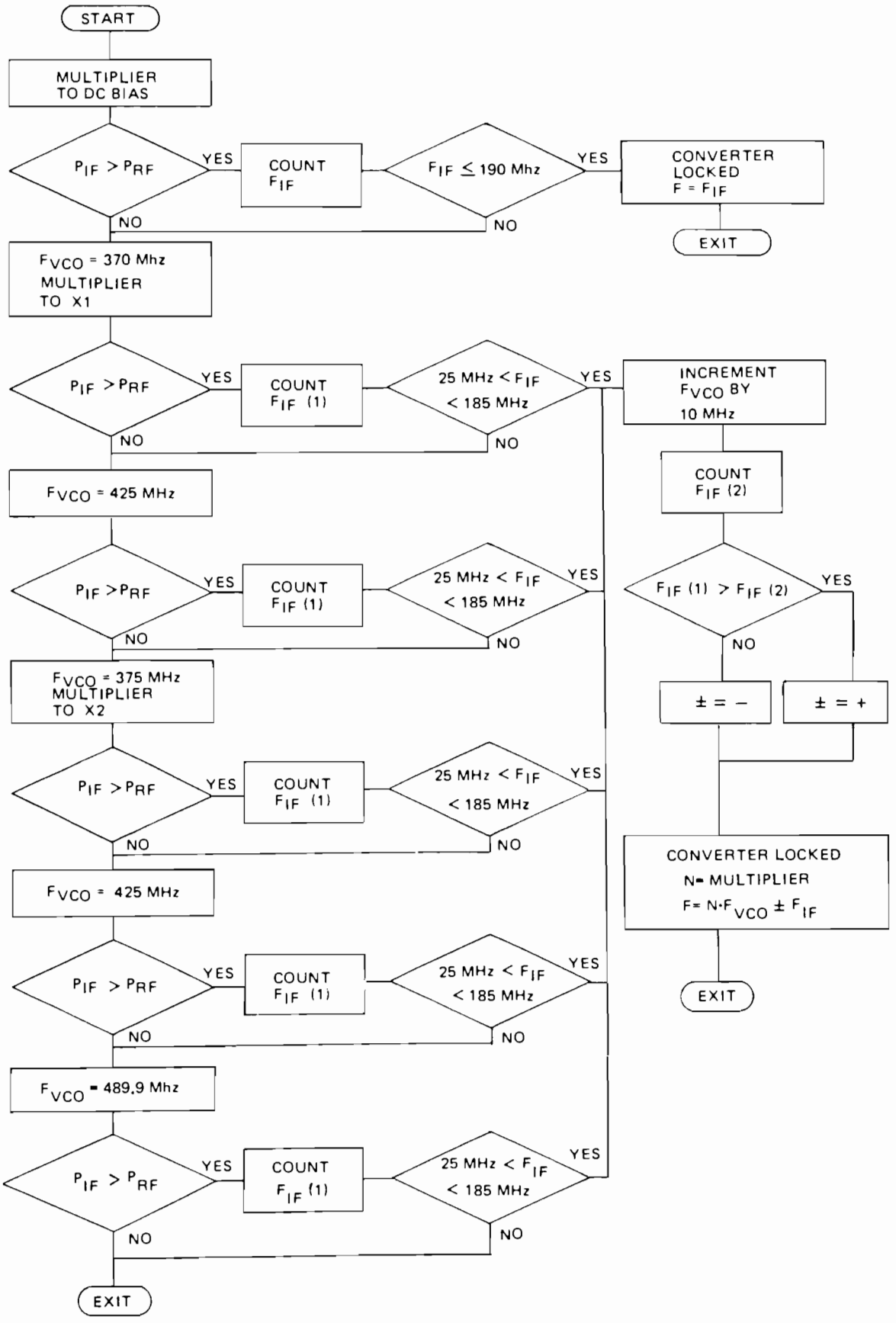


Figure 4-3. Band 2 Converter Operation

The L.O. frequencies being used, except the range of direct counting (< 190 MHz), have been selected so only IF frequencies from 25 MHz to 185 MHz are required. Since the counter can count signals less than 10 MHz, the restricted operating range provides margin for frequency modulation on the input signal, and for incrementing the VCO frequency.

Figure 4-4 shows the operating ranges for the various harmonics and VCO frequencies used.

Input Frequency Range F_{IN}(MHz)	VCO Frequency F_{VCO}(MHz)	Harmonic Number N	IF Frequency Range F_{IF}(MHz)
10 - 190	–	0	10 - 190
185 - 345	370	1	185 - 25
345 - 400	425	1	80 - 25
400 - 560	375	1	25 - 185
560 - 610	425	1	135 - 185
610 - 725	375	2	140 - 25
725 - 825	425	2	125 - 25
825 - 935	375	2	75 - 185
935 - 1035	425	2	85 - 185
1035 - 1164.8	489.9	2	55.2 - 185

Figure 4-4. Band 2 Operating Ranges

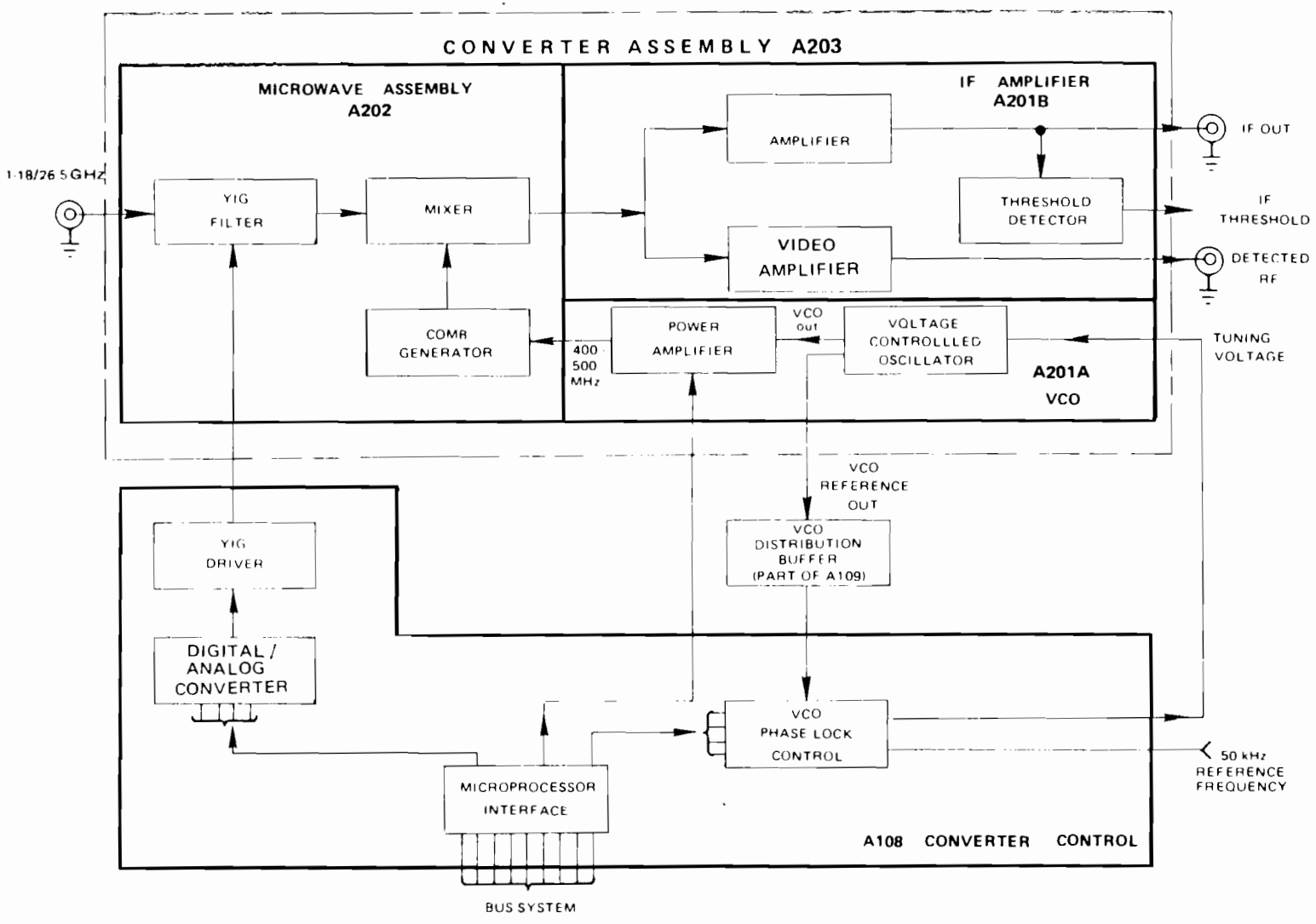


Figure 4-5. Band 3 Converter, Simplified.

BAND 3 CONVERTER

Measurement of a signal in Band 3 is accomplished by down converting from the microwave range to approximately 127 MHz. This is accomplished by mixing the input signal with a known reference frequency, which is found by selecting a VCO harmonic in the range of 400 to 500 MHz. The VCO frequency can be selected in 50 kHz increments by using a microprocessor controlled phase lock system, while retaining the accuracy and stability of the counter's time base reference.

A simplified diagram of the Band 3 converter is shown in figure 4-5. There are two major assemblies. The Converter Control assembly (A108) and the Converter Assembly (A203).

CONVERTER CONTROL A108

The Converter Control assembly contains the interface between the microprocessor bus system and the Converter (A203). A digital-to-analog converter and a precision current (YIG) driver provide a 2 MHz frequency resolution for setting the YIG filter of A202.

A108 also contains the programmable VCO phase lock control system. This system lets the microprocessor interface select any VCO frequency between 400 and 500 MHz, in increments of 50 kHz.

CONVERTER A203

The Converter assembly consists of three subassemblies.

- A201A, Voltage Controlled Oscillator (VCO) assembly
- A201B, IF Amplifier Assembly
- A202, Microwave Assembly (YIG)

The A202 Microwave Assembly contains the YIG filter, mixer and comb generator.

The input signal (1 GHz - 20 GHz/26.5 GHz) passes through a YIG filter on A202. The filter is an electronically tunable bandpass filter, with an operating frequency proportional to its tuning current. This filter determines the approximate frequency of the input signal and filters out any undesired signals, making it possible to count a signal at one frequency even if a larger signal is present at another frequency.

When tuning the YIG filter to the input signal, the mixer is used as an RF detector, and its output is amplified in the video amplifier on the IF assembly.

The output of the Video amplifier is maximum when the YIG filter is tuned to the input signal. In the case of multiple input signals, the video amplifier output determines which signal is largest.

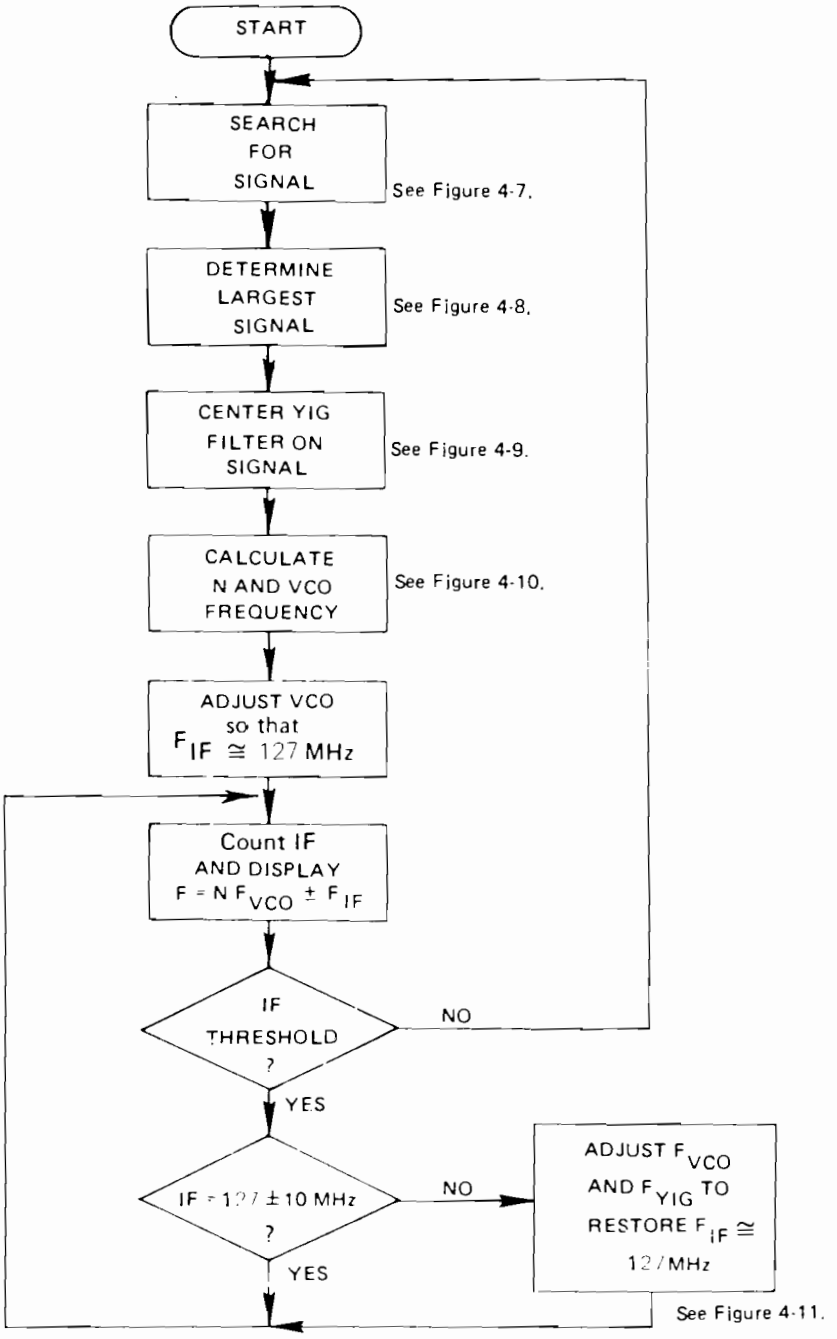


Figure 4-6. Band 3 Operation, Simplified.

Once the YIG filter is tuned to the input signal, the appropriate harmonic number (N) and VCO frequency (F_{VCO}) are selected to produce an IF frequency (F_{IF}) at approximately 127 MHz. An approximation of the input signal is found by using:

$$F_{IN} = N F_{VCO} \pm F_{IF}$$

The IF frequency produced in the mixer is amplified by the high gain IF amplifier and sent to the Count Chain (A106). The IF threshold detector (A201B) insures sufficient IF amplitude for count accuracy.

OPERATION

First the YIG filter is stepped, (in 64 MHz steps), from its low to high limits. During this search the RF detected output is fed, through a microprocessor controlled step attenuator to a threshold detector. After each step the threshold detector is checked. If triggered, the search mode is halted until the amplitude of the signal is determined. This is done by stepping the filter back and forth through the signal and stepping the attenuator until the signal is attenuated below the threshold. The counter then returns to the search mode to look for any larger signals. After searching the entire frequency range, it returns to the largest signal and begins to center the YIG filter precisely on the input frequency. See Figure 4-6 for a simplified diagram of Band 3 operation. For more detailed descriptions of Band 3 operation see Figures 4-7 through Figure 4-11.

The centering process consists of slowly stepping the YIG filter down (in 2 MHz increments) until a level of 3-6 dB below the peak is reached. This frequency is stored and the process is repeated from the other side by stepping the filter up in 2 MHz steps. The average of the two frequencies obtained is the center of the passband. This is the frequency which is used to determine the N and F_{VCO}.

After centering, N is determined from $N = \frac{F_{YIG} - 127}{500}$ and then rounded up to the next highest integer.

From this, F_{VCO} is calculated using $F_{VCO} = \frac{F_{YIG} - 127}{N}$ Should this yield $F_{VCO} < 400$ MHz, then F_{VCO} is recalculated using $F_{VCO} = \frac{F_{YIG} - 127}{N}$.

Since F_{YIG} is only approximately equal to F_{IN}, the IF frequency will not be exactly 127 MHz. Therefore, the next step in operation is a VCO frequency adjustment to shift F_{IF} into the middle of the IF passband.

VCO frequency correction is achieved by counting F_{IF} and changing F_{VCO} by $\pm \frac{F_{IF} - 127}{N}$. If the error is large enough to be outside the IF passband (IF threshold is not triggered) then a series of steps (shifting the IF in $\pm$ 20 MHz increments) are taken until the signal falls within the passband.

Once the VCO corrections have been made, the converter has acquired the signal and the counter is ready to count and display the input frequency.

After each measurement, the frequency of the IF is examined. If the input frequency has shifted more than 10 MHz, new frequencies for the YIG and VCO are calculated to restore the IF to 127 MHz. This method provides rapid tracking of a signal being tuned.

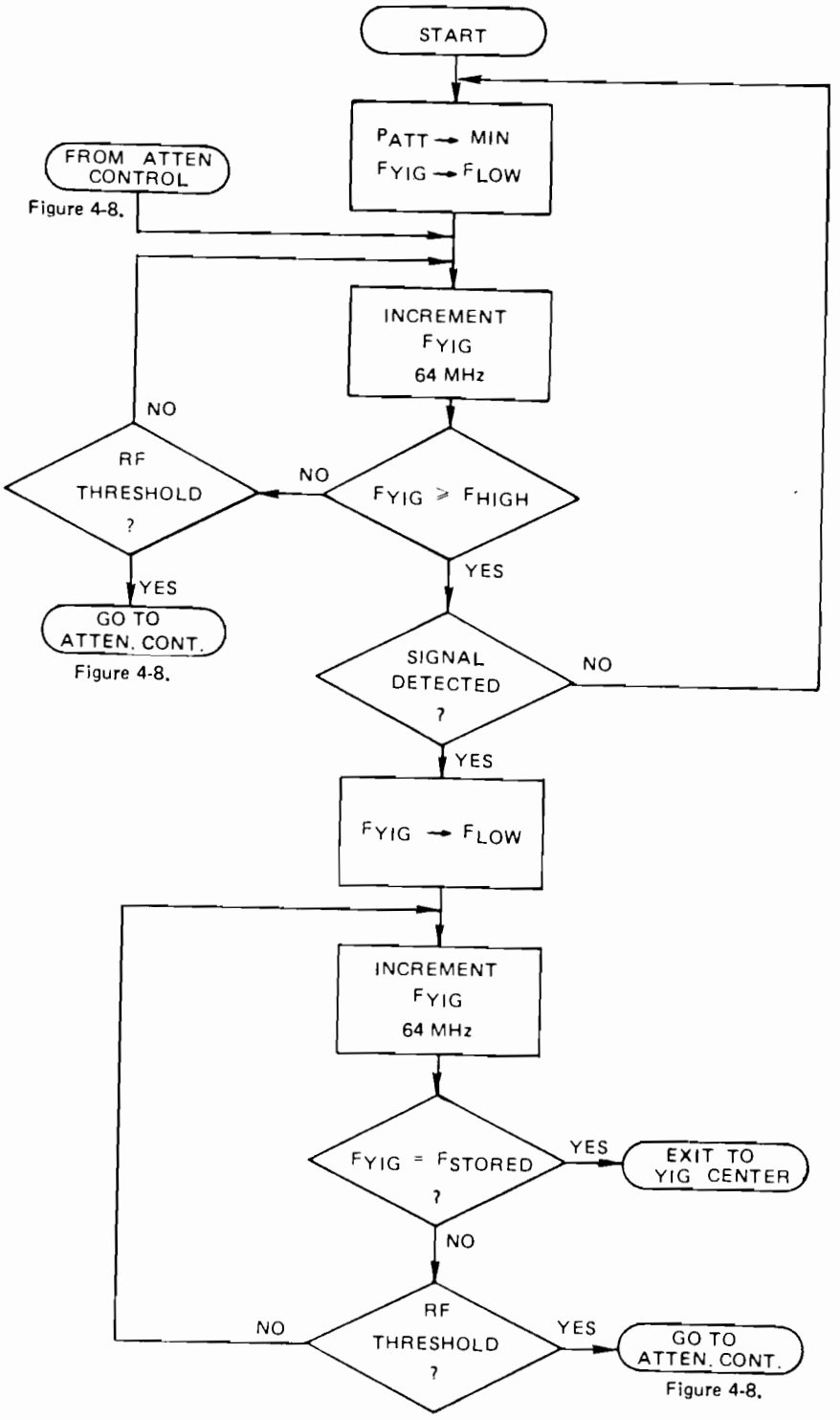


Figure 4-7. Band 3 Search For Signal

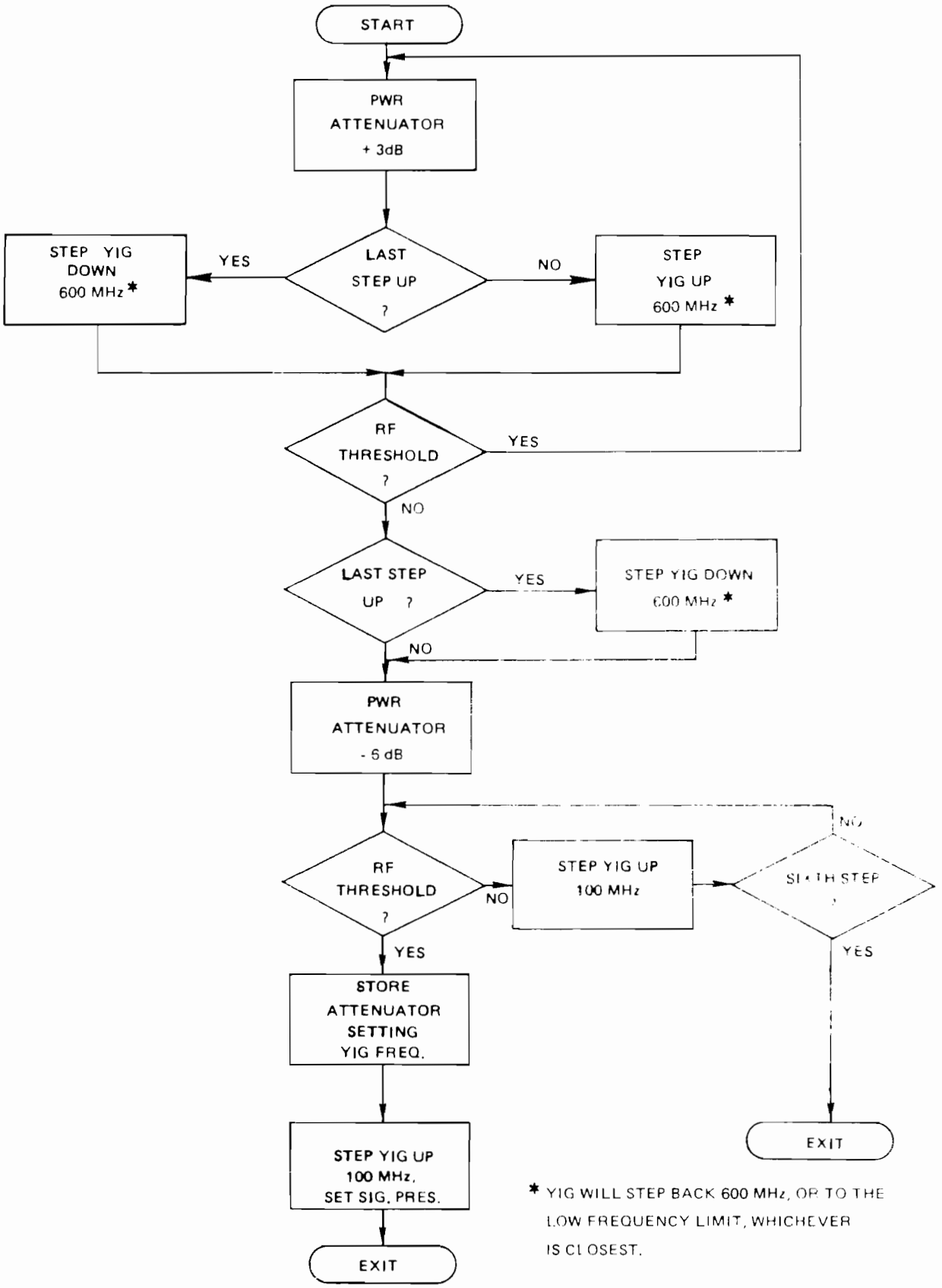


Figure 4-8. Determine Largest Signal

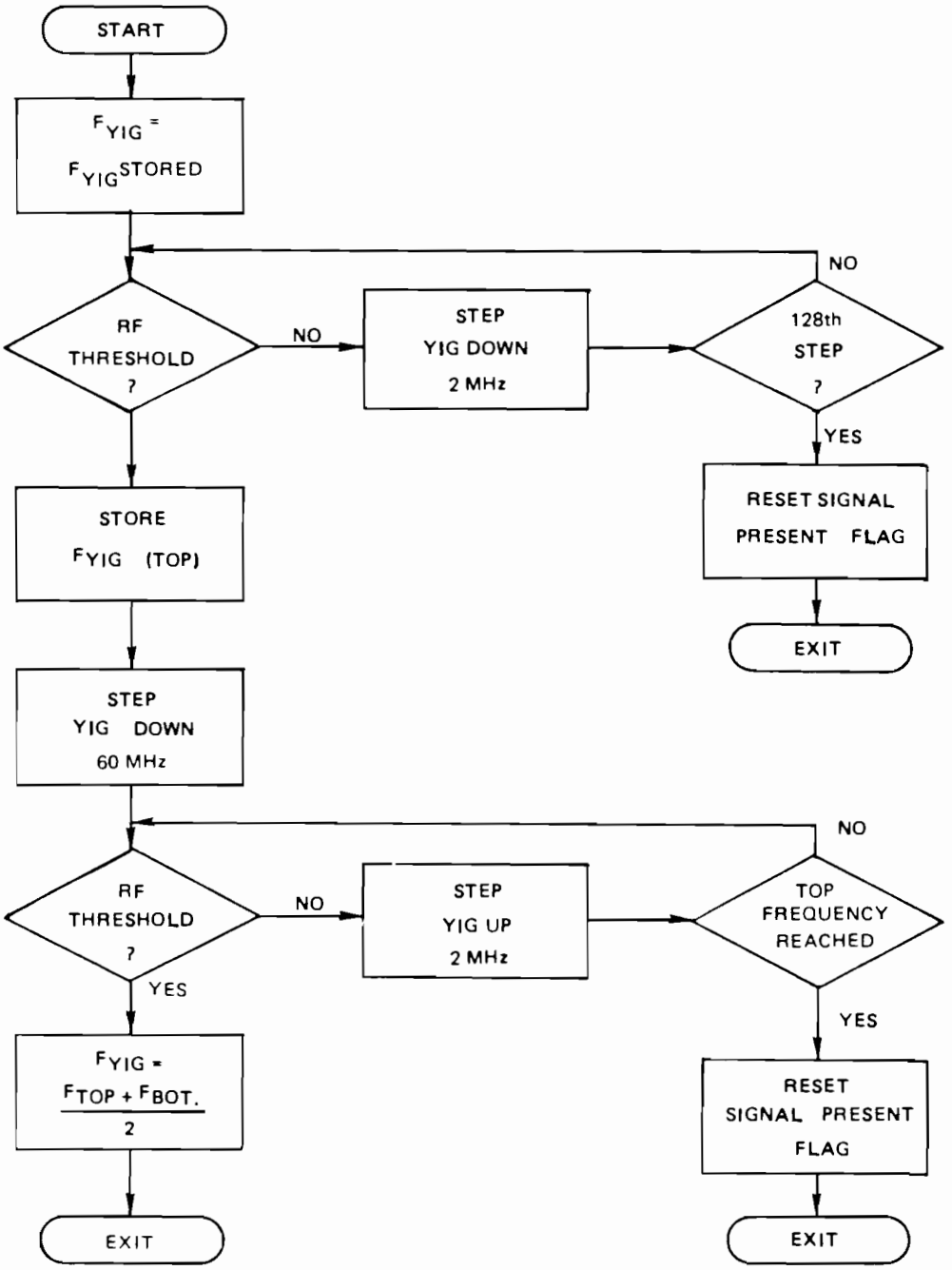


Figure 4-9. YIG Centering

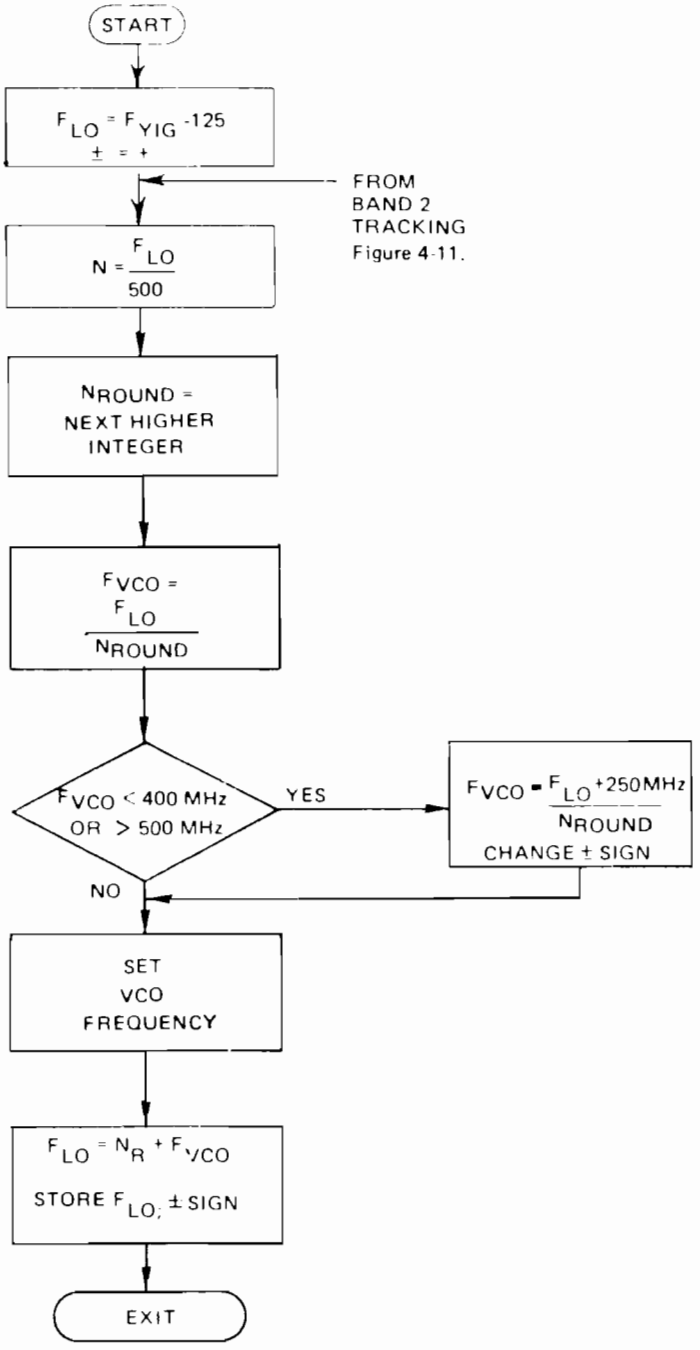


Figure 4-10. Calculate N and VCO Frequency

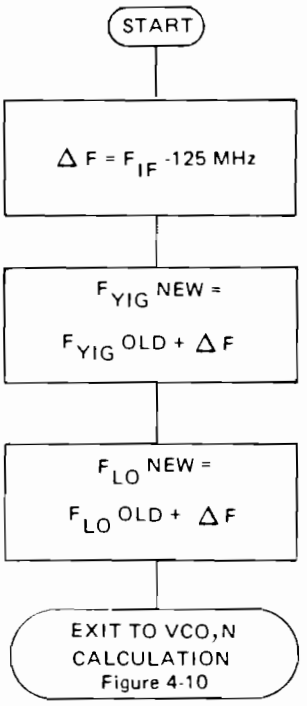


Figure 4-11. Band 3 Signal Tracking

Section 5
Maintenance and Service

This section contains instructions and information to maintain your counter.

FUSE REPLACEMENT

The counter uses one fuse. It is located on the rear panel next to the voltage select switch.

- For 100/120VAC operation use a 1.0A slow-blow MDL type fuse.
- For 220/240VAC operation use a 0.50A slow-blow FST type fuse.

The voltage select switch should be set to the proper line voltage. To change line voltage:

1. Be sure the counter is disconnected from the power line.
2. With a flat edged screwdriver, rotate the voltage select switch until the arrow points to the desired line voltage.
3. Change to a fuse with the value specified for the line voltage selected.

NOTE:
Always be sure that the fuse is the type and value specified for, and that the voltage select switch is set to correspond to the AC power input voltage, or the counter may be damaged.

AIR CIRCULATION

Air circulates through the vents in the rear panel of the counter. These vents must not be obstructed or the temperature inside the counter may increase enough to reduce the counter stability and shorten the component life.

PERIODIC MAINTENANCE

No periodic preventive maintenance is required. To maintain accuracy, it is recommended that the counter be recalibrated every six months.

CAUTION

Do not attempt repair or disassembly of the Microwave Converter or Time Base Oscillator Assemblies. Contact EIP or your sales representative.

If the following assemblies are repaired or replaced the counter may require recalibration for proper operation.

- Power Supply, A101
- Gate Generator, A107
- Converter Control, A108
- Microwave Converter, A203

Care should be taken when removing any assemblies to prevent damage to components or cables.

FACTORY

If the counter is being returned to EIP for service or repair, be sure to include the following information with the shipment.

- Name and address of owner.
- Model and complete serial number of counter.
- A COMPLETE description of problem (Under what conditions did problem occur? What was the signal level? What equipment was attached or connected to the counter? Did that equipment experience failure symptons?)
- Name and telephone number of someone familiar with the problem that may be contacted by EIP for any further information, if necessary.
- Shipping address to which the counter is to be returned. Include any special shipping instructions.
- Pack the counter for shipping (Refer to Section 2).

FIELD

EIP has an assembly exchange program. All plug in assemblies, modules, and the front panel assembly may be exchanged.

After identifying the faulty assembly, call EIP with the assembly number and shipping information. A replacement will be shipped within 24 hours. After the replacement assembly has been received, return the faulty assembly to EIP for credit.

Section 6
Troubleshooting

This section defines troubleshooting aids that are incorporated in the 535 /538 counter. They are.

- Signature analysis
- Self diagnostics
- Keyboard controlled circuit tests

The procedures and tables are provided for troubleshooting to a functional circuit level.

SIGNATURE ANALYSIS

Signature analysis is a technique used to troubleshoot complex logic circuitry. It uses data compression to reduce any data pattern to a 4 character alpha-numeric word.

The start and stop inputs define the measurement window. Each time a transition within the measurement window occurs on the clock input, the probe is sampled, and the logic level is shifted into the analyzer. This information is used to generate a signature unique to that data string. That signature can then be compared to a reference signature, taken from a known good product, to determine if the data string is correct.The counter implements signature analysis in either a free running or program controlled manner.

FREE RUNNING

This mode of signature analysis is essential for troubleshooting problems that could prevent the program from running. A CLRB instruction can be forced by breaking the data bus at A105 JMP1 and grounding A105 TP5, effectively "free running" the microprocessor. "Free running" means forcing a simple instruction (such as NOP or CLRB) on the data bus, which the microprocessor sees at every address location. This causes the microprocessor to continually cycle through its entire address range, accessing everything on the address bus as it does. By strategically placing the start and stop connections the entire bus system can be probed for bad signatures.

	START	STOP	CLOCK
CONNECTIONS	A105 TP4	A105 TP4	A105 TP3
BUTTONS	IN	IN	IN

LINE	SIGNATURE
A0 (P1 Pin 54)	UUUU
A1 (P1 Pin 54)	FFFF
A2 (P1 Pin 53)	8484
A3 (P1 Pin 51)	P763
A4 (P1 Pin 50)	1U5P
A5 (P1 Pin 49)	0356
A6 (P1 Pin 48)	U759
A7 (P1 Pin 47)	6F9A
A8 (P1 Pin 46)	7791
A9 (P1 Pin 45)	6321
A10 (P1 Pin 44)	37C5
A11 (P1 Pin 43)	6U28
A12 (P1 Pin 42)	4FCA
A13 (P1 Pin 41)	4868
A14 (P1 Pin 40)	9UP1
A15 (P1 Pin 39)	00001
U3 Pin 7	76AC
U5 Pin 8	0000
TP6	854F
TP7	PACH
TP8	755F
TP9	755H
U8 Pin 19	U3P7
U9 Pin 18	0003
U10 Pin 18	0003
U17 Pin 1	9F14
U17 Pin 12	9F17

+ 5V 0003, phase 2 0003 *

* Due to the synchronous qualities of the signature analyzer, phase 2 will read the same as + 5V but the logic probe will be flashing. Likewise, anything gated with phase 2 may have the same signature as the ungated signal.

Figure 6-1. Microprocessor Free Running Signatures

PROGRAM CONTROLLED

If the counter is working sufficiently to access the test functions, program controlled signature analysis can be used. In program controlled signature analysis the start and stop (and therefore the signature) are controlled by software. This allows the signature analyzer to be used, in many cases, to troubleshoot the hardware outside the bus system.

SELF DIAGNOSTICS

At turn on the counter performs several internal diagnostic checks, checking the RAM, PROM, and the associated decoding circuitry. The display shows dashes during these checks. If the counter passes the tests it then enters the normal operating mode. If it fails RAM check the display will show all Es and a unique signature will be generated. If the counter fails any of the PROM checks an error message will be displayed, and a signature will be generated. Please refer to Figure 6-2.

The counter generates PROM error signatures only during the power up diagnostics check. It is necessary to turn the power off, and then on again while the signature analyzer is connected to get a signature.

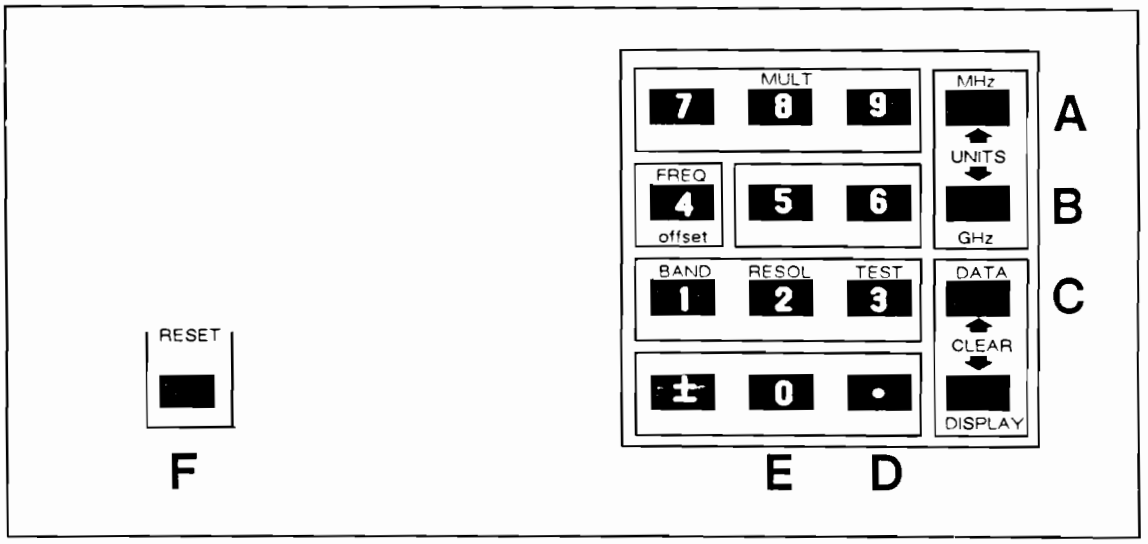
	START	STOP	CLOCK	PROBE
CONNECTION BUTTONS	A106 TP5 OUT ↑	A106 TP5 IN ↓	A105 TP8 IN ↓	A105 TP6 (+5V)

PROBLEM	ERROR	SIGNATURE
Ram Bad	All E's	007U
A105 U13 (Basic Program) Bad	31	1UFP
A105 U17 (Basic Program) Bad	32	U399
A105 U15 (Basic Program) Bad	33	P672
A105 U17 (GPIB or BCD/RMT) Bad	36	8AFH

Figure 6-2. Self Diagnostic Error Indications

KEYBOARD CONTROLLED CIRCUIT TESTS

There are 10 keyboard controlled circuit tests (01 thru 10). All tests are accessed by pressing TEST and then the two digit test number. Tests which do not require keyboard inputs to function (tests 01 02, 03, 04, 06, 07) can be exited by pressing any key. The counter will exit the test and enter the functions selected. Tests which use the keyboard in their operation (tests 05, 08, 09, 10) can be exited by pressing any key not used by the test. All tests can be exited by pressing CLEAR DISPLAY. The counter will return to normal operation. Some tests require hexadecimal coded keyboard inputs (tests 08, 09, 10). For those tests the keyboard is defined in Figure 6-3.



KEY	HEX EQUIV.	KEY	HEX EQUIV.
0	0	9	9
1	1	MHz	A
2	2	GHz	B
3	3	CLR DATA	C
4	4		
5	5	•	D
6	6	+/–	E
7	7	RESET	F
8	8	CLR DISPLAY	EXITS TEST

Figure 6-3. Keyboard Configuration For Tests Requiring Hexadecimal Inputs.

	START	STOP	CLOCK	PROBE
CONNECTION	OUT ↑	IN ↓	IN ↓	
BUTTONS	A106 TP5	A106 TP5	A105 TP8	A105 TP6 (+5V)

BUTTON	COORDINATES	SIGNATURE
Reset	47	U68C
7	41	A19C
8	42	66PU
9	43	CCH7
MHz	44	U5PU
4	31	PUPH
5	32	UC70
6	33	HF3A
GHz	34	OPA2
1	21	APH1
2	22	C45H
3	23	1766
CLR DATA	24	H9C8
+/–	11	375U
0	12	H7PC
•	13	UAHH
CLR DISPLAY	EXIT TEST	C75U

Figure 6-4. Keyboard Test Coordinates and Signatures.

TESTS

01 **200 MHz Self Test** This test sets the VCO to 400 MHz, divides it by two, and counts the 200 MHz output from the divider. It checks the count chain, VCO and VCO phase lock circuitry, and the gate generator.

02 **8s Test** This will light all LED s, annunciators, and decimal points. It checks that everything on the display is lit, the intensity of the display, and the alignment of the LED s and annunciators.

03 **Display Segment Test** This lights one segment of each digit and one annunciator at a time, cycling through all segments. The cycle rate can be adjusted with the sample rate pot. It verifies that each segment of the display, segment drivers, and display multiplexer operate properly and independently.

04 **Display Digit Test** This lights one entire digit and its decimal point at a time. It cycles through all digits and annunciators. The cycle rate is determined by the sample rate pot. It checks each digit and digit driver independently and verifies operation of the display multiplexer.

05 **Keyboard Test** This will display the coordinates of each key as it is pressed. It also generates a unique signature for each key, so the keyboard can be checked without the display. Test 05 may be entered by keyboard or by momentarily tying A108 TP1 to A105 TP6. This makes it possible to enter the keyboard test for troubleshooting even if the keyboard is not operating well enough to enter the test in a normal manner. Test 05 checks the keyboard, keyboard interrupt, and keyboard decode circuitry. The coordinates and signatures for each key are shown in Figure 6-4.

06 **Converter Ramp Test** Test 06 continuously ramps the Band 3 Converter DAC from 0 to 27 GHz, in 2 MHz (LSB) steps. It also generates a signature for each of the inputs to the DAC. (See Figure 6-5). It can be used to test the YIG DAC, YIG drivers, YIG, and Band 3 RF level circuits.

	START	STOP	CLOCK
CONNECTIONS	A106 TP5	A106 TP5	A105 TP8
BUTTONS	OUT ↑	IN ↓	IN ↓

NODE	SIGNATURE	NODE	SIGNATURE
A108 U4 Pin 2	9U78	A108 U4 Pin 9	7763
A108 U4 Pin 3	9946	A108 U4 Pin 10	HP8A
A108 U4 Pin 4	8F62	A108 U4 Pin 11	P45A
A108 U4 Pin 5	89U9	A108 U4 Pin 12	80A8
A108 U4 Pin 6	833F	A108 U4 Pin 13	77U6
A108 U4 Pin 7	U9CC	A108 U4 Pin 14	7245
A108 U4 Pin 8	FCA6	A108 U4 Pin 15	28U9
+ 5V	49P4		

Figure 6-5. Converter Ramp Test Signatures

07 VCO Test This test cycles the VCO frequency from 400 to 500 MHz, in increments of 50 kHz. The cycle rate can be adjusted by the sample rate pot. 07 tests the VCO and the phase lock circuitry. This test operates only when the counter is in Band 2 or Band 3

10 Information Read/Alter Routine Test 10 can read any microprocessor address and, if that address is RAM or I/O, change its contents. The desired address is entered as a 4 digit hexadecimal number (see Figure 6-5). When the fourth digit is entered, the counter will display the contents of the desired address. The contents are then changed by entering a two digit hexadecimal number.

NOTE

Test 10 can change any temporary storage in the counter, including locations that are essential to the operation of the counter. Changing the wrong location will not damage the counter permanently, but it can cause improper operation. To return the counter to proper operation turn the counter off then back on.

SIGNIFICANT ADDRESSES, I/O PORTS

If an I/O bit is configured as an output, the number read by test 10 will be the same number that is programmed. If an I/O bit is configured as an input, the number read by test 10 will be the input signal level on the I/O line. Therefore, if an I/O port is programmed, and then read, the number displayed may not correspond to the number programmed because some bits of the I/O port may be configured as inputs.

DESCRIPTION	ADDRESS OF PA PORTS	ADDRESS OF PB PORTS
PIA on Count Chain (A106)	AC00	AC02
PIA on Gate Generator (A107)	9900	9902
Frequency Control PIA on Converter Control A108	9840	9842
Programmable Counter PIA on Converter Control (A108)	9820	9822
PIA on Band 2 Converter (A109)	9880	9882
PIA on Front Panel Logic (A111)	9808	980A

DESCRIPTION	ADDRESS
GPIB Address Switch	9C04

Figure 6-6. I/O Addresses.

Two important I/O port locations are the YIG frequency control (address 9840, 9842) and the VCO frequency control (address 9820, 9822).

To convert from the desired YIG frequency to the PIA program number: *

1. Round the desired frequency to a multiple of 2 MHz (The YIG D.A.C resolution is 2 MHz)
2. Divide the desired frequency in MHz by 2 (F/2).
3. Convert F/2 from decimal to hexadecimal.
4. The two most significant digits are programmed to address 9842, and the two least significant digits are programmed to address 9840.

To convert from the desired VCO frequency to the PIA program number:

EXAMPLE (420.75 MHz)

1. Round the desired frequency to a multiple of 50 kHz
   (The resolution of the VCO frequency is 50 kHz).
2. Multiply the desired frequency (in MHz) by 5 . . . . . 420.75 X 5 = 2103.75
3. If the result contains no fractional part, go to step 8.
4. Multiply only the fractional part by 16 . . . . . .75 X 16 = 12
5. Add the result to the most significant digit from step 2. . . . . .MSD of 2103.75 = 2 · 2 + 12 = 14
6. Convert the result to hexadecimal . . . . . $14_{10} = E_{16}$
7. Replace the MSD from step 2 with the result from step 6
   and drop the fractional part. . . . . 2103.75 → E103
8. The two most significant digits are programmed to address 9822, and the two least significant digits are programmed to address 9820.

* The counter must be in Band 2 or Band 3 to perform this function.

SIGNIFICANT ADDRESSES, RAM

All storage in RAM are in the following formats.

REGISTER FORMAT, FREQUENCY STORAGE		
ADDRESS	SIGN (00 = + , FF = –)	
ADDRESS + 1	100 GHz	10 GHz
ADDRESS + 2	1 GHz	100 MHz
ADDRESS + 3	10 MHz	1 MHz
ADDRESS + 4	100 KHz	10 KHz
ADDRESS + 5	1 KHz	100 Hz
ADDRESS + 6	10 Hz	1 Hz

REGISTER FORMAT, POWER STORAGE		
ADDRESS	SIGN (00 = +, FF = –)	
ADDRESS + 1	NOT	USED
ADDRESS + 2	NOT	USED
ADDRESS + 3	NOT	USED
ADDRESS + 4	NOT	USED
ADDRESS + 5	100 dB	10 dB
ADDRESS + 6	1 dB	. 1 dB

REGISTER	ADDRESS
L.O. frequency	01A8
I.F. frequency	023F
Frequency output to display	01B8
Frequency limit low	025B
Frequency limit high	0254
Frequency offset	0246

Figure 6-7. Frequency Storage Registers

REGISTER	ADDRESS
Power output to display	01BF
Power offset	024D

Figure 6-8. Power Storage Registers

TROUBLESHOOTING TREES

Troubleshooting trees are intended only as a guide, and do not describe every possible failure situation. Turn power off before removing or installing any P.C. boards or connectors. If the following assemblies are repaired or replaced, recalibration of the counter will be necessary.

- A101 Power Supply
- A107 Gate Generator
- A108 Converter Control
- A203 Converter Assembly

CAUTION

Do not attempt to repair or disassemble
the A203 hybrid assembly.

TEST EQUIPMENT REQUIRED

MANUFACTURER	MODEL	DESCRIPTION	CRITICAL PARAMETERS
Tektronix	475	Oscilloscope	100 MHz min. Bandwidth
Fluke	8050A	D.V.M.	4½ digit resolution
H.P.	182C, 8559A	Spectrum Analyzer	125 MHz
H.P.	5004A	Signature Analyzer	
H.P.	651B	Signal Generator	10 Hz - 10 MHz
Wavetek	2002	Sweeper	10 MHz - 2 GHz
EIP	931	Microwave Source	1 GHz - 20 GHz
H.P.	8690A, 8696A	Microwave Sweeper	18 GHz – 26.5 GHz

Figure 6-9. Troubleshooting Test Equipment (Or Equivalent).

To use the troubleshooting trees:

1. Refer to the main troubleshooting tree.

2. Step through the main troubleshooting tree, performing all necessary checks, until the failure mode is noted.

3. Refer to the appropriate troubleshooting tree for that failure mode.

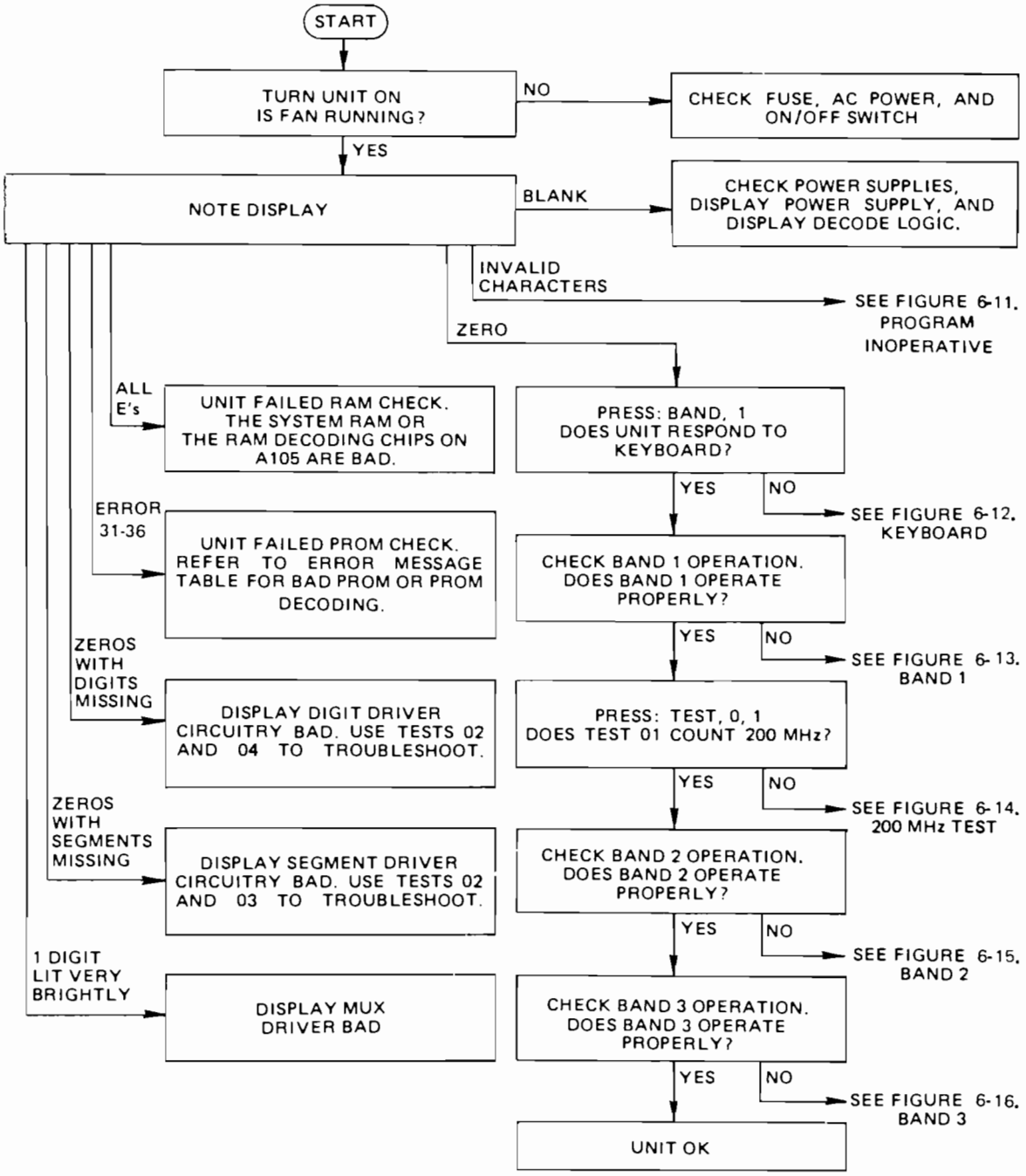


Figure 6-10. Main Troubleshooting Tree

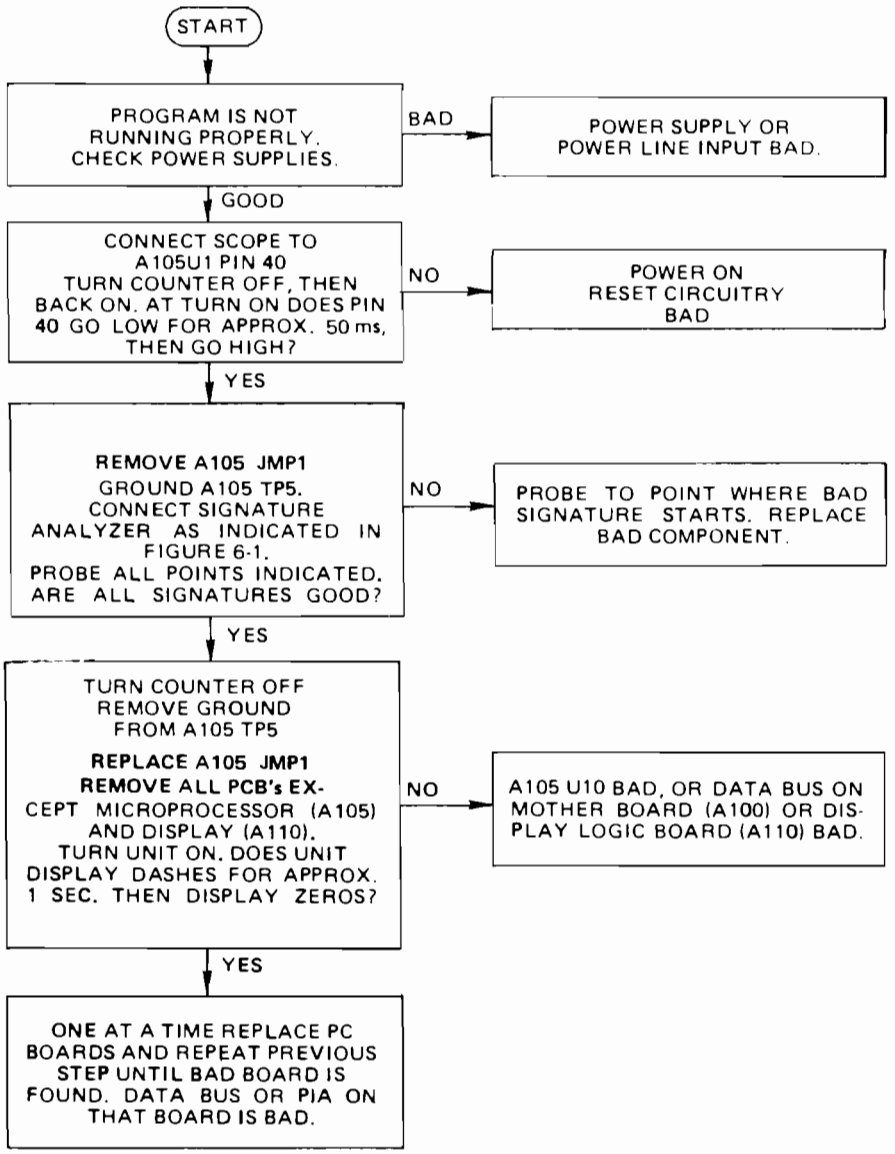


Figure 6-11. Program Inoperative

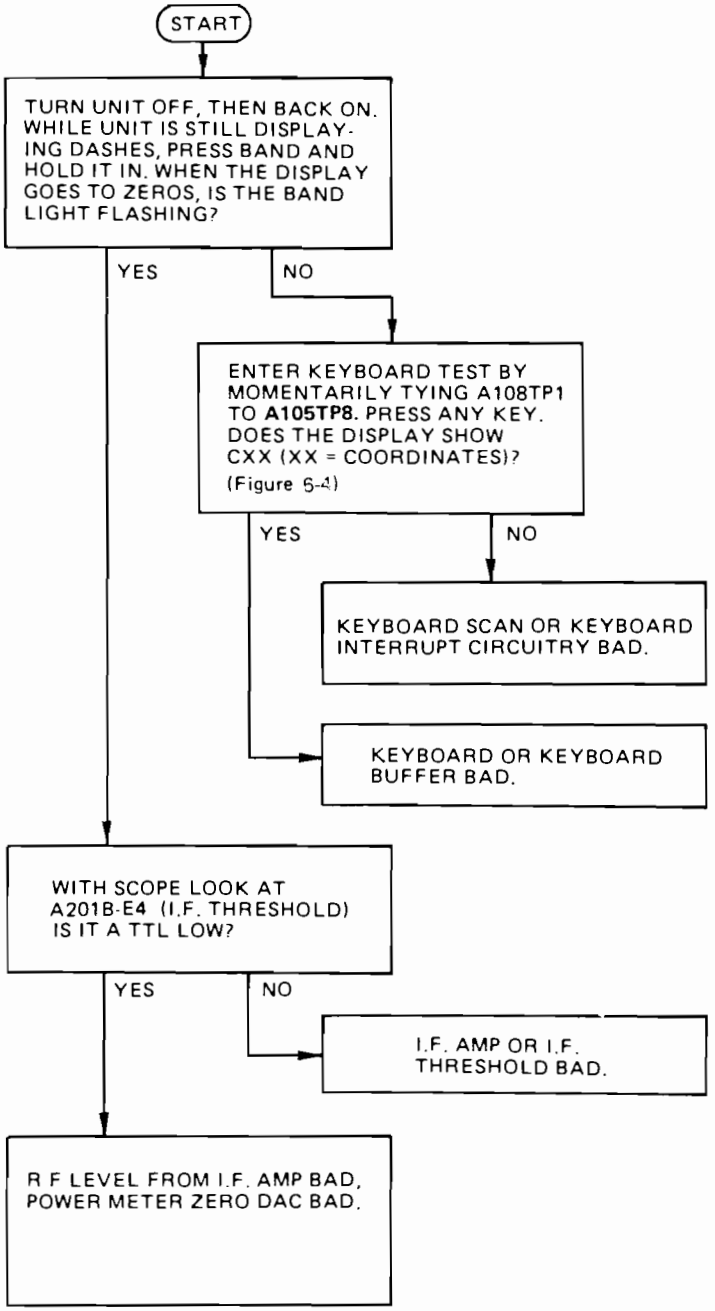


Figure 6-12. Keyboard

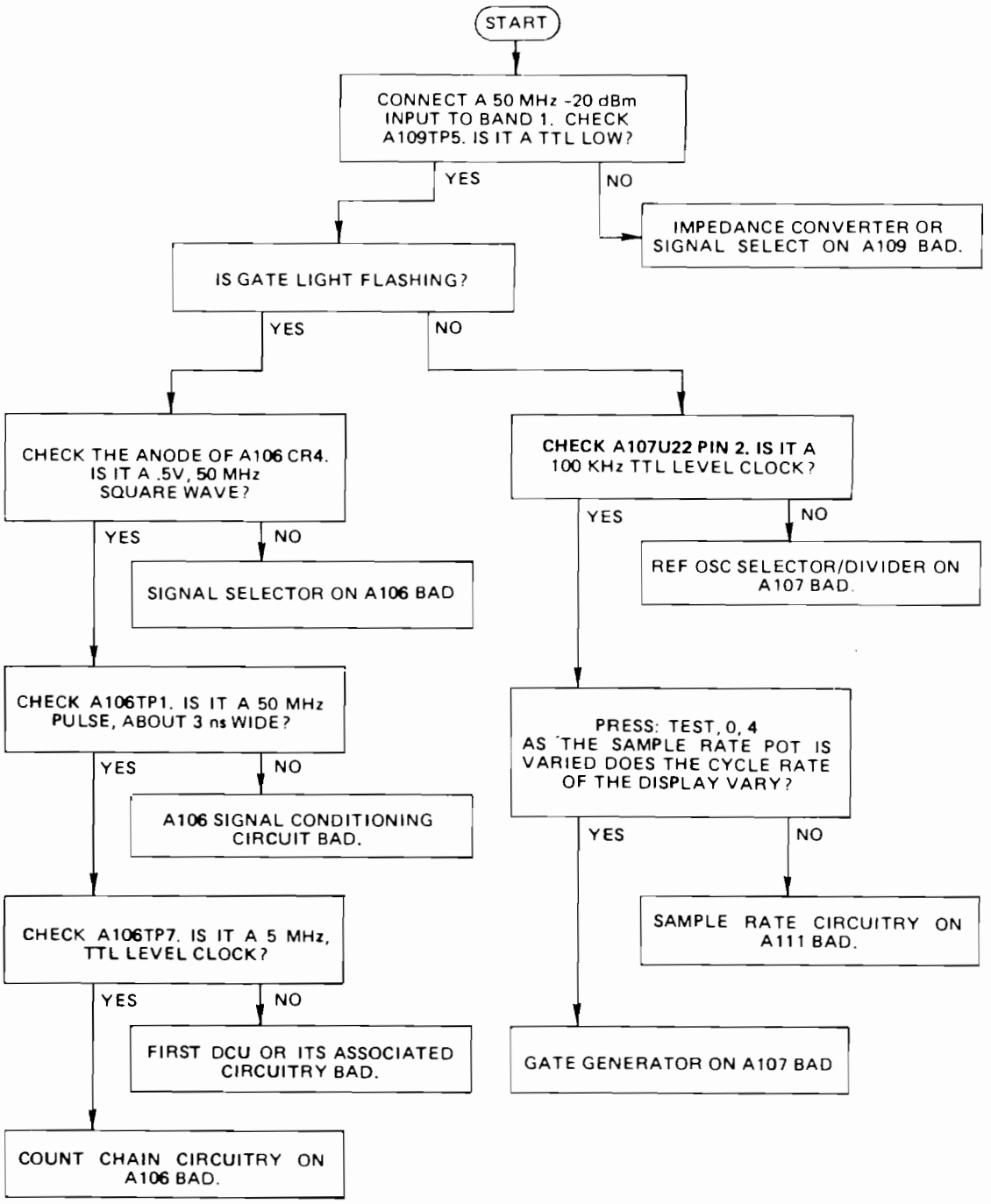


Figure 6-13. Band 1

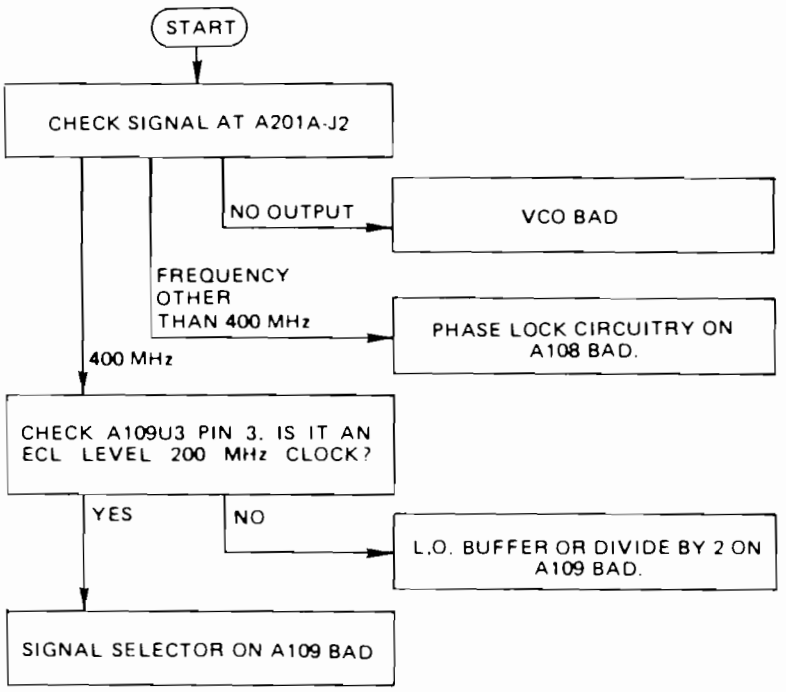


Figure 6-14. 200 MHz Test

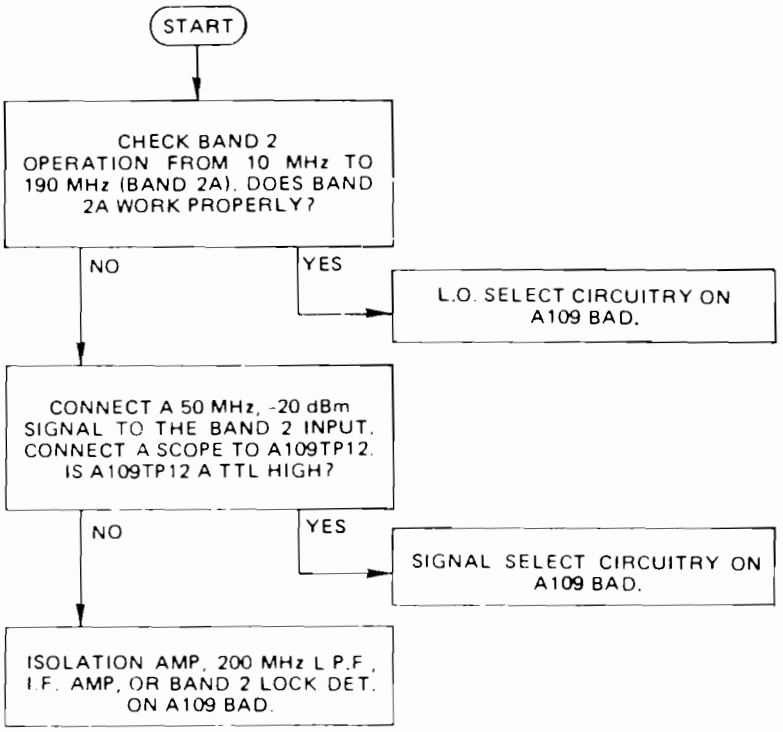


Figure 6-15. Band 2

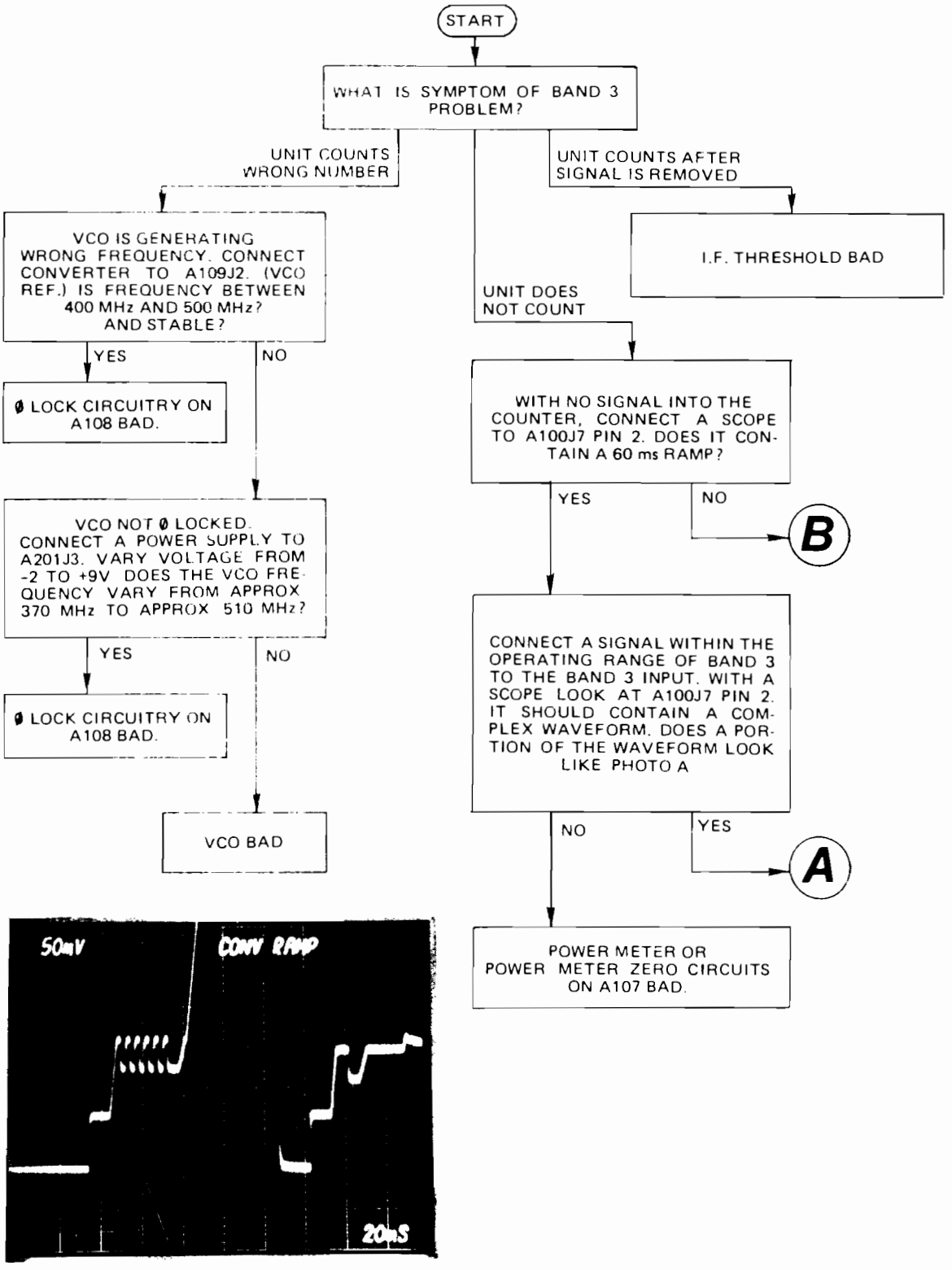


PHOTO A

Figure 6-16 Band 3

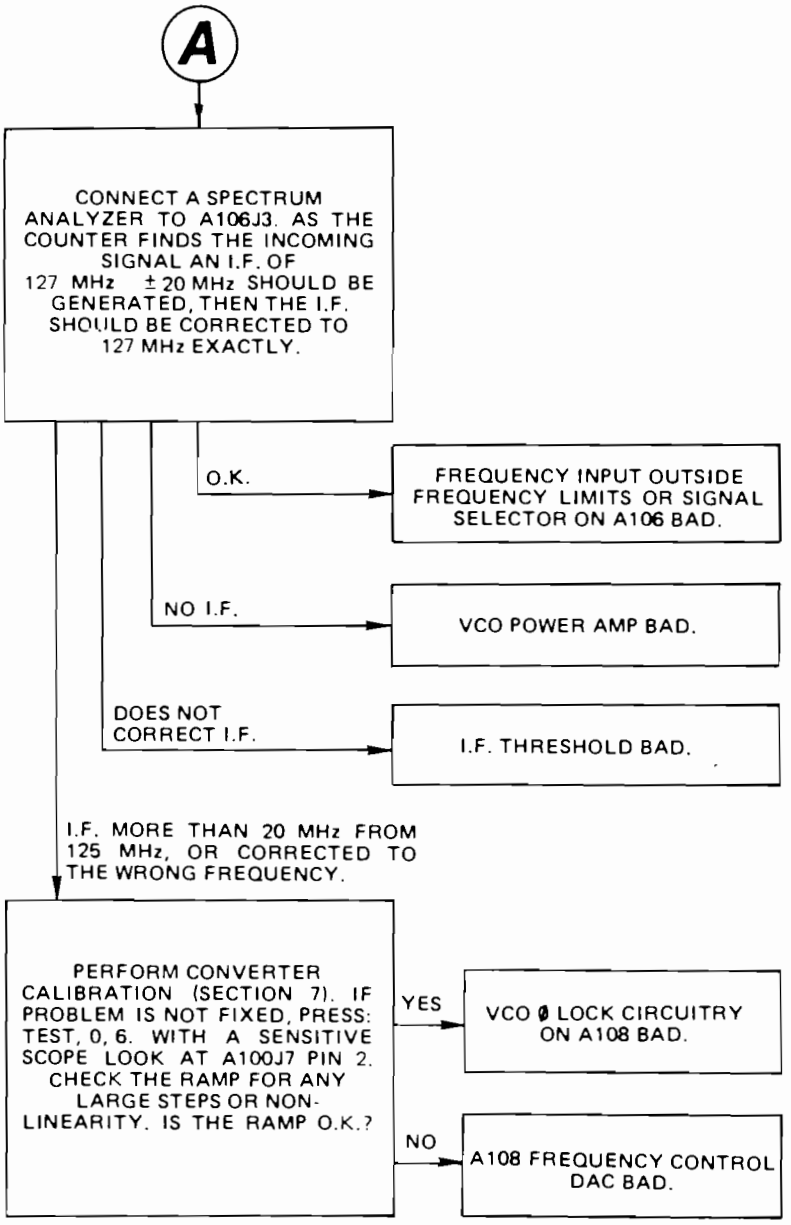


Figure 6-16. Band 3, continued

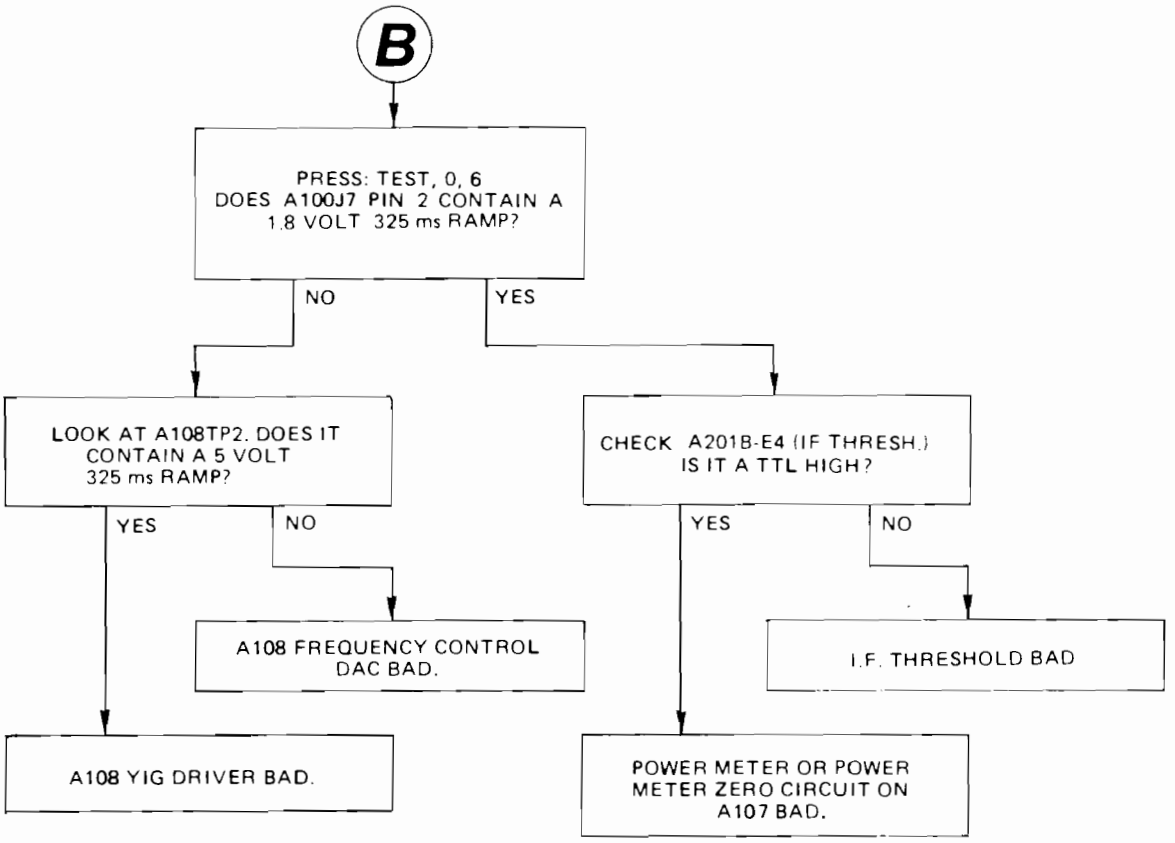


Figure 6-16. Band 3, continued

Section 7
Adjustments and Calibrations

GENERAL

To adjust the 535B or 538B counter correctly, use the following procedures. Adjustments should only be made if the counter does not operate as specified, or following the replacement of components. If the adjustments do not result in the performance specified, then refer to the troubleshooting section of this manual. The test equipment required is:

MANUFACTURER	MODEL	DESCRIPTION	CRITICAL PARAMETERS
Tektronic	475	Oscilloscope	General Purpose
Fluke	8050A	D.V.M.	41/4 digit resolution
H.P.	182C, 8559A	Spectrum Analyzer	125 MHz
Wavetek	2002	Sweeper	10 MHz - 2 GHz
EIP	931	Microwave Source	1 - 20 GHz
H.P.	8690A, 8696A	Microwave Sweeper	18 GHz - 26.5 GHz
EIP	2000017	Service Kit	See Appendix A (A-1)

POWER SUPPLY ADJUSTMENTS

Prior to making any adjustments to the power supply the counter should warm up at least 20 minutes.

Voltages are measured on the back of tne Power Supply board (A101).

1. Connect the Digital Volt Meter (DVM) between ground and +12V on A101, pin 1 and 8.
2. Adjust A101 R5 until the voltage measures +12.000 VCD ± .010 VDC.
3. Connect the DVM between ground and -12 V on XA101, pin 1 and 18.
4. Adjust A101 R17 until the voltage measures -12.000 VDC ± .010 VDC.

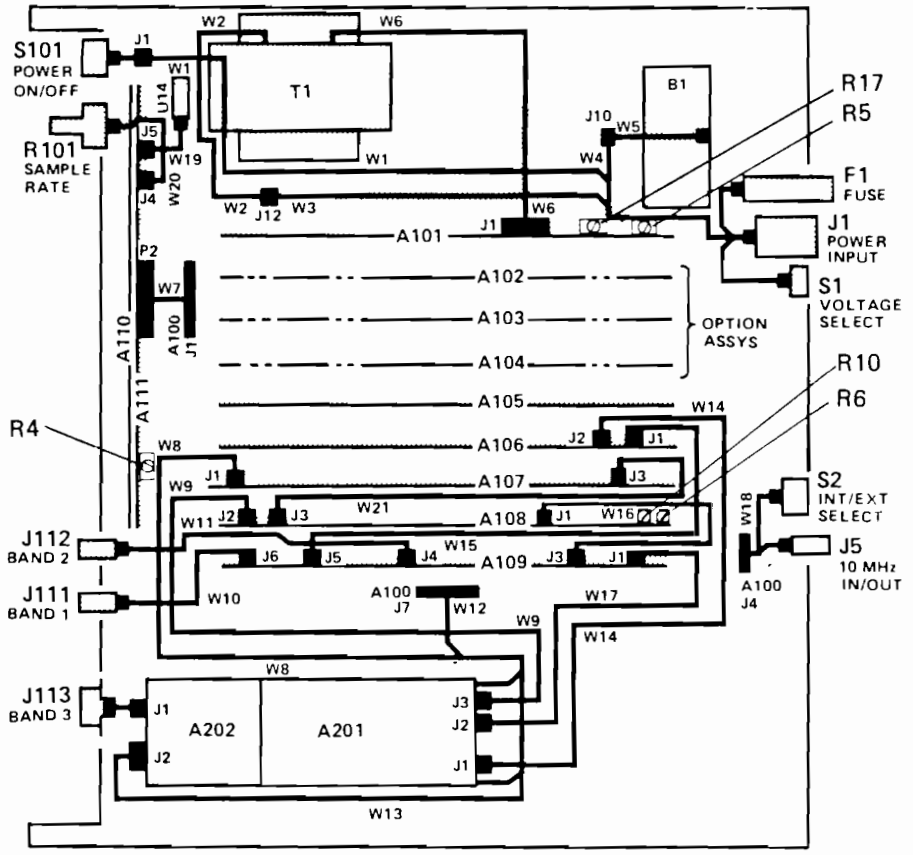


Figure 7-1. Adjustment Locations.

YIG DAC CALIBRATION PROCESS

THEORY

The purpose of this process is to compensate the nonlinearity of the YIG and DAC error. The process allows a software route start in the EEPROM. The instrument generates a YIG DAC correction table, which resides in EEPROM. After the YIG searches for and centers on a signal, the software corrects the DAC reading (not the DAC itself) according to the correction table. This process yields the true YIG frequency. Then the program tunes the VCO according to the true YIG frequency instead of the ERROR DAC reading.

Each entry of the correction table contains two values:

(1) the YIG frequency and
(2) the DAC reading

Each value consists of 2 bytes. The YIG frequency is represented in hex in 2 MHz increments. For example, if the YIG frequency is 1 GHz then:

1 GHz = 1000 MHz = 2 * 500 MHz = 2 * 01F4 (hex)

and "01F4" is what is written to the table.

The table looks like this:

entry 1	YIG freq 1	DAC reading 1*
entry 2	YIG freq 2	DAC reading 2
. . .	. . .	. . .
. . .	. . .	. . .
entry N	YIG freq n	DAC reading n*

where N must be **at least 2 and can be as much as 248.** *The values in entry 1 and N are extrapolated.

YIG DAC CORRECTION TABLE

Given a DAC reading D, the software first searches through the second row of the table. If D is equal to an exact DAC reading in entry n, where 1 <= n <= 248, then the software generates the corresponding YIG frequency reading. If D falls between 2 consecutive DAC readings in entry p and q, where 1 < = p < q < = 248, then the software uses a linear interpolation algorithm to find the corresponding YIG frequency Y as shown in the following equation:

If:
$$\frac{\text{DAC q} - \text{DAC p}}{\text{YIG q} - \text{YIG p}} = \frac{\text{D} - \text{DAC p}}{\text{Y} - \text{YIG p}}$$

then Y is:

$$Y = (D - DAC\ p) * \frac{YIG\ q - YIG\ p}{DAC\ q - DAC\ p} + YIG\ p$$

NOTE

When Y is being calculated, the multiplication is performed before the division to avoid precision error.

If for some reason the instrument cannot find a suitable DAC reading entry, ERROR #40 is generated to indicate error in the correction table.

CORRECTION TABLE SETUP

Setting up the correction table is actually the YIG DAC calibration process. The user enters "Test 90" to activate the process. At first the table contains two entries:

	YIG frequency	DAC number
default 1	0	0 hex
default 2	3FFF hex	3FFF hex

The user applies a synthesized signal Y1 GHz to the counter, then enters Y1 GHz through the counter's front panel or via GPIB. After the user enters the number, a routine converts that number to hexadecimal, stores it to the table as the YIG frequency of entry #2, and shifts the original entry #2 to entry #3. Then the counter sweeps the YIG to look for the signal and center the YIG on it. If the searching and centering are successful, the DAC number D1 is read and stored as DAC # of entry #2 of the table. Now the table looks like this:

default 1	0	0
entry 1	Y1	D1
default 2	3FFF	3FFF

The user can repeat the above sequence up to 246 times with the following restrictions:

(1) the sequence must be repeated at least two times.

(2) the frequency entered must be greater than the previous frequency.

If either of the two requirements above are not fulfilled or the counter cannot center the YIG on the signal, the whole process is aborted and the correction table is not altered.

After N repetitions, the correction table will be as follows:

default 1.	0	0
entry 1.	Y1	D1
entry 2.	Y2	D2
. . .	. . .	. . .
entry N-1.	Y N-1	D N-1
entry N.	YN	DN
default 2.	3FFF	3FFF

where 2 <= N <= 246.

Since default values are used for the first and the last entry, they must be corrected before the user exits the calibration process. The software accomplishes this task by using Y1, Y2, D1, D2 to extrapolate default 1 and Y N-1, YN, D N-1, DN to extrapolate default 2.

The equation is :

$$Y = \frac{D \cdot (Y2 - Y1) + Y1 \cdot D2 - Y2 \cdot D1}{D2 - D1}$$

The final correction table looks like this:

extrapolated entry 0.	Y0	D0
entry 1.	Y1	D1
entry 2.	Y2	D2
. . .	. . .	. . .
entry N-1	Y N-1	D N-1
entry N	YN	DN
extrapolated entry N+1	Y N+1	Y N+1

where 2 <= N <= 246.

FORMAT AND ADDRESS OF THE CORRECTION TABLE

The correction table resides in EEPROM.

Address: 0C00 hex

Format:

yyyy dddd yyyy dddd .... yyyy dddd FFFF FFFF EEEE

where "yyyy" means 2 bytes of YIG frequency
"dddd" means 2 bytes of DAC reading
"FFFF FFFF" represents 4 bytes of end of table mark and
"EEEE" means for software usage.

NOTE

Before performing this procedure A108 S-1 must be open. (A108 U4 Pin 17 will be high). After calibration, S1 must be on (A108 U4 P17) low to protect calibration.

CALIBRATION PROCEDURE

Manual Calibration

1. Press "BAND 3" on the front panel.
2. Press "TEST 90" on front panel. the counter will then display "F01".
3. Apply a synthesized 1-GHz signal at 0 dBm to Band 3 of the counter.
4. Enter "1" and press "GHz" on the front panel.
5. Counter should display "F02".
6. Apply a synthesized 1.3-GHz signal at 0 dBm to Band 3 of the counter.
7. Enter "1", ".", "3" and press "GHz" on the front panel.
8. Counter should display "F03".
9. Apply a synthesized 10-GHz signal at 0 dBm to Band 3 of the counter.
10. Enter "1", "0" and press "GHz" on the front panel.
11. Counter should display "F04".
12. Apply a synthesized 20-GHz signal at 0 dBm to Band 3 of the counter.
13. Enter "1", "8" and press "GHz" on the front panel.
14. Counter should display "F05".
15. **Go to step 28 if the model of the counter is 535B/535B/575B.**
16. Apply a synthesized 22-GHz signal at 0 dBm to Band 3 of the counter.
17. Enter "2", "2" and press "GHz" on the front panel.

18. Counter should display "F06".
19. Apply a synthesized 24-GHz signal at 0 dBm to Band 3 of the counter.
20. Enter "2", "4" and press "GHz" on the front panel.
21. Counter should display "F07".
22. Apply a synthesized signal 25.5 GHz at 0 dBm to Band 3 of the counter.
23. Enter "2", "5", ".", "5" and press "GHz" on the front panel.
24. Counter should display "F08".
25. Apply a synthesized signal 26.5 GHz at 0 dBm to Band 3 of the counter.
26. Enter "2", "6", ".", "5" and press "GHz" on the front panel.
27. Counter should display "F09".
28. Press **"CLEAR DATA"** to abort the process, or press **"CLEAR DISPLAY"** to exit the process.

NOTE:

If the counter can not find or center on the signal, it will display an ERROR #42 message.

NOTE:

The above frequencies are required to calibrate the counter. Other frequencies are at user's choice.

Calibration using GPIB controller.

1. Output "B3TA90" to the counter.
2. Command the signal source to generate 1 GHz at 0 dBm.
3. Output "1G" to the counter.
4. Command the signal source to generate 1.3 GHz at 0 dBm.
5. Output "1.3G" to the counter.
6. Command the signal source to generate 10 GHz at 0 dBm.
7. Output "10G" to the counter.
8. Command the signal source to generate 20 GHz at 0 dBm.
9. Output "18G" to the counter.
10. **Go to step 19 if the model of the counter is 535B/535B/575B.**
11. Command the signal source to generate 22 GHz at 0 dBm.
12. Output "22G" to the counter.

13. Command the signal source to generate 24 GHz at 0 dBm.
14. Output "24G" to the counter.
15. Command the signal source to generate 25.5 GHz at 0 dBm.
16. Output "25.5G" to the counter.
17. Command the signal source to generate 26.5 GHz at 0 dBm.
18. Output "26.5G" to the counter.
19. Output "C" to exit the calibration process or "D" to abort the process.

NOTE:

When the counter has acquired the signal and is ready to accept the next frequency, the GPIB status byte bit 0 will be set to 1. This can be recognized through service request.

TIME BASE CALIBRATION

It is important to note that the precision of the time base calibration directly affects overall counter accuracy. Reasons for recalibration, and the procedures to be used, should be thoroughly understood before attempting any readjustment.

The fractional error in the frequency indicated by the counter is equal to the negative of the fractional frequency error of the Time Base Oscillator with respect to its true value. That is:

$$\frac{\Delta f_s}{f_s} = \frac{\Delta f_t}{f_t}$$

where f_s is the true frequency of the measured signal, and f_t is the true frequency of the Time Base Oscillator. Thus, the inaccuracy associated with a frequency measurement is directly related to the quality of the Time Base Oscillator, and a measure of the precision with which it was originally adjusted.

TEMPERATURE COMPENSATED CRYSTAL OSCILLATOR (TCXO)

The standard time base oscillator used in the counter is a TCXO (A113). The range of the actual measured frequencies of the oscillator will differ by no more than 1 parts in 10^6 if the temperature is slowly varied from 0 to +50 degrees C.

With a stable input frequency, the measurement indicated by the counter will fluctuate in proportion to the TCXO drift. To center this fluctuation on the true value of the measured signal, each TCXO has imprinted on its side the frequency setting required at +25 degrees C.

At approximate room temperature (+25 degrees C), the slope of the frequency vs. temperature curve is normally no worse than $\pm 1 \times 10^{-7}$ parts per degree C. When the counter is used in an ordinary laboratory environment, the TCXO may be set as close to 10,000,000 Hz as desired. In this environment, a peak-to-peak temperature variation of 5^0 C will result in a measured signal error of no more than $\pm$ 2.5 X 10^{-7} parts. This signal error is due to the temperature characteristics of the time base oscillator.

The natural aging characteristics of the crystal in the time base oscillator can also cause inaccurate signal measurements. Aging refers to the long term, irreversible change in frequency (generally in the positive direction) that all quartz oscillators experience. The magnitude of this frequency fluctuation in the TCXO is less than 3 X 10^{-7} parts per month as specified. This may improve to at least 1 X 10^{-6} parts per year when in continuous operation.

Error due to aging adds directly to error due to temperature. The number of times the counter requires recalibration depends on the environment in which the counter operates, and upon the level of accuracy required.

For example, if the counter is subjected to the full operation temperature range one month after proper initial adjustments, the inaccuracy could vary from +1.3 X 10^{-6} parts to -0.7 X 10^{-6} parts.

TCXO CALIBRATION PROCEDURES

METHOD 1 (with accurate frequency counter)

1. Remove top cover of counter. Connect counter to reliable power source. Note ambient temperature.

2. Measure the frequency of the TCXO (at the rear panel 10 MHz connector) with a second counter of known calibration accuracy.

3. Adjust the TCXO by turning the calibration screw on the TCXO case until the measured frequency equals that shown on the TCXO calibration label.

METHOD 2 (with accurate frequency source)

1. Apply a 10 000 000 Hz signal from a frequency standard (or other oscillator of suitable accuracy and stability) to the Band 1 input of the counter.

2. Press RESOL [ ] [0] (1 Hz resolution)

3. Adjust the TCXO until the reading on the counter is offset from 10 000 000 Hz by the negative of the frequency shown on the TCXO. For example, if the TCXO calibration label shows a frequency of 10 000 003 Hz, adjust the TCXO until the counter displays 9 999 997 Hz.

DISPLAY INTENSITY

On the front panel logic assembly (A111) R4 may be adjusted to provide the most comfortable display intensity.

Section 8
Performance Tests

GENERAL

These tests are for the basic counter. Performance tests for options are in Section 10. These tests will enable the user to verify that the counter is operating within specifications.

VARIABLE LINE VOLTAGE

During the performance tests the counter should be connected to the power source, through a variable voltage device, so that line voltage may be varied ±10% from nominal. This will assure proper operating of the counter under various supply conditions.

REQUIRED TEST EQUIPMENT (or equivalent)

MANUFACTURER	MODEL	DESCRIPTION	CRITICAL PARAMETERS
H.P.	651B	Signal Generator	10 Hz - 10 MHz
Wavetek	2002	Sweeper	10 MHz - 2 GHz
EIP	931	Microwave Source	1 GHz - 20 GHz
H.P.	8690A, 8696A	Microwave Sweeper	18 GHz - 26.5 GHz

BAND 1 (10 Hz - 100 MHz)

1. Set the counter to Band 1.
2. Connect the signal source output, through a 50 ohm shunt feedthrough resistor, to the Band 1 input on the counter.
3. Set the signal level to 25 mv RMS (-19 dBm into 50 ohms).
4. Vary the signal from 10 Hz to 100 MHz (changing signal source as required).

The counter should display the correct input frequency.

BAND 2
(10 MHz - 1 GHz)

1. Set the counter to Band 2.
2. Connect the signal source output to the Band 2 input of the counter.
3. Set the signal level to -15 dBm.
4. Vary the signal input from 10 MHz to 1 GHz.

The counter should display the correct input frequency.

BAND 3
(535B: 1 GHz - 20 GHz)
(538B: 1 GHz - 26.5 GHz)

1. Set the counter to Band 3.
2. Connect the signal source output to the Band 3 input of the counter.
3. Vary the signal frequency from 1 GHz to 20/26.5 GHz (changing the signal source as required) at the following levels.

1.0 GHz - 12.4 GHz	-25 dBm (7 mv RMS)
12.4 GHz - 20 GHz	-20 dBm (12 mv RMS)
20 GHz - 26.5 GHz	-15 dBm (38 mv RMS)

The counter should display the correct input frequency.

Section 9
Functional Description and Illustrated Parts Breakdown

This section contains a functional description, a parts list, an illustration, and a schematic diagram for each printed circuit board used in this counter.

Parts are listed alphabetically by component type and then in numeric order within component type. Components that have a different reference designator (REF DES) but the same EIP part number are described for the first such component listed. Subsequent descriptions of that component will refer to the first entry. The total number of like components used on the same assembly will be listed with the first entry in the column identified as UNITS PER ASSEMBLY.

The last two columns of the parts list give the name and the Federal Supply Code for Manufacturers (FSCM) numberof the manufacturer. A list of manufacturers' names, addresses, and FSCM numbers is given in Appendix B. The FSCM number is used in the parts list as a guide to the manufacturer or supplier of a part.

Pages 9-3 through 9-5 contain the top assembly of the counter and other basic information. After page 9-5, the page numbers have a three-digit first number followed by a dashed number. The three-digit number reflects the number of the assembly being described on those pages. The dashed number is the page sequence for the description on that assembly. For example, pages 105-1 through 105-5 all relate to the A105 printed circuit board. This page numbering system facilitates simple, modular page replacement when an assembly revision makes a manual update necessary.

REFERENCE DESIGNATORS

A	Assembly	J	Jack or Connector	S	Switch
B	Battery or Fan	K	Relay	T	Transformer
C	Capacitor	L	Inductor	TP	Test Point
CR	Diode	P	Plug or PCB Contacts	U	Integrated Circuit
DS	Indicator (Display)	Q	Transistor	X	Socket or Holder
F	Fuse	R	Resistor	Q1-3	Q1 through Q3
				Q1/2	Q1 and Q2 (matched pair)

ABBREVIATIONS

CBN	CARBON	NOM	Nominal
CER	Ceramic	PC	Printed Circuit
CMT	Cermet	PCB	Printed Circuit Board
CNTR	Counter	pF	picofarad
CONV	Converter	PREC	Precision
COMP	composition	PROM	Programmable Read Only Memory
CONN	Connector	RAM	Random Access Memory
ELEC	Electrolytic	RSTR	Resistor
FDTH	Feedthrough	RT AN	Right Angle
FLM	Film	S.A.T.	Value or type selected at factory test. Part may not be used.
FML	Female		
GP	General Purpose	SW	Switch
IC	Integrated Circuit	TANT	Tantalum
K	Kilo (x 1,000)	TRIM	Trimmer
LED	Light Emitting Diode	uF	Microfarad
M	Meg(a) (x 1,000,000)	uH	Microhenry
MET OX	Metal Oxide	VAR	Variable
MF	Metal Film	WPRF	Waterproof
mH	Millihenry	WW	Wirewound
ML	Male	XSTR	transistor
MTCH PR	Matched Pair		

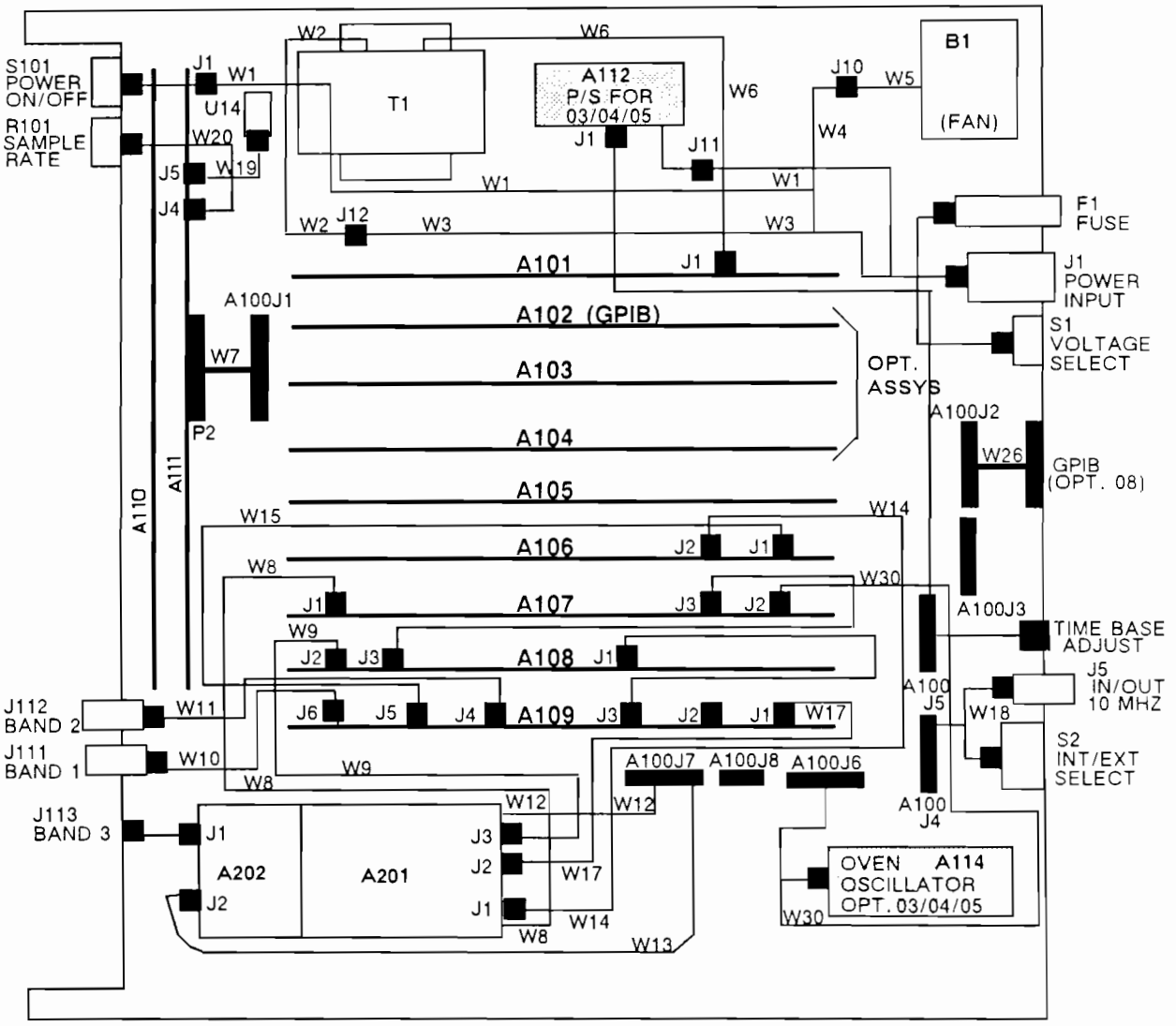


Figure 9-1. Assembly Locations and Cable Connections in 535B/538B Counter

CABLE CONNECTION GUIDE

FROM	CABLE	TO
A1S101J1	W1	A1S1, F1,J1
A1J12	W2	A1T1
A1S1	W3	A1J12
A1J10	W4	A1S1
A1B1	W5	A1J10
A101J1	W6	A1T1
A111P2	W7	A100J1
A107J1	W8	A201A
A108J2	W9	A201J3
A1J111	W10	A109J6
A1J112	W11	A109J4
A201	W12	A100J7)

FROM	CABLE	TO
A202J2	W13	A100J7)
A106J2	W14	A201J1)
A106J1	W15	A109J5
A108J1	W16	A109J3
A109J1	W17	A201J2
A1J5,S2	W18	A100J4
A1U14	W19	A111J5
A1R101	W20	A111J4
A107J3	W21	A108J3
A100J2	W26	A1,GPIB (OPT. 08)
107J2	W30	A100J6 (OPT. 03/04/05)

535B/538B MICROWAVE COUNTER

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
	COUNTER, MODEL 575B	2000014-03		EIP	34257
	MODEL 578B	2000015		EIP	34257
	FRONT PANEL ASSY (535B)	2010673-01	1	EIP	34257
-1	**FRONT PANEL ASSY (538B)**	5210673-01	1	EIP	34257
	Knob, Knurled	5210223	1	5000160	31013
	Switch, Power	2010187-02	1		
	Button Set, 12 + 9	5210220	1	5230005-02	
	Panel	5210378-01	1		
	Sample Rate Control Assy	2010134-01	1		
	Alignment Pin	5210190	2		
	Retainer Key	5210191	1		
	Front Panel Overlay	5210543-02			
		5210555-02			
-2	**REAR PANEL ASSY**	2010219-01	1	EIP	
	Panel	5210379	1		
	Conn. Filter	2650005	1	3EF1	05245
	Switch, Toggle SPDT,120V,5A	4510001	1	7101H	09353
	Fuse Holder	5000170	1	031-1653/1666/1663	
	Fuse, 1A, SB, 250V	5000085	1	MDL-1A	71400
	Fuse Carrier	5000171	1	FST034-3114	71400
	Conn, BNC	2610024	1	KC-79-35	91836
	Voltage Select Switch Assy,A151	2010159-01	1		
-3	**FAN ASSY**	2010136-02	1		
	Fan	5000151	1	760/126LF/182/1115	
	Conn, Plug, 3 Pin	2620110	1	03-06-2032	0000A
	Contact, Male	2620038	2	02-06-2103	0000A
	Spacer	5210404	2		
-4	**FRAME KIT**	2010151-02	1		
	Panel, Side, Enclosure	5210312	2		
	Trim, Front Post	5220004	2		
	Trim, Handle	5220025	2		
	Frame	5210248	2		
	Corner Post, Front	5210311	2		
	Corner Post, Rear	5250002	2		
	Handle, Enclosures	5250011	2		
-5	**TRANSFORMER, ASSY, A1T1**	2010359-01	1		
	Transformer, Power	4900005	1		
	Conn, Plug, 9 pin	2620112	1	03-06-2092	0000A
	Conn, Housing, 6 pin	2620129	Ref	640427-6	AMP
	Contact, Male	2620038	7	02-06-2103	0000A
	Contact, Female	2620036		02-06-1103	0000A
-6	**FRONT CARD GUIDE ASSY**	5210199	1	5210199-7	
-7	**REAR CARD GUIDE ASSY**	5210200	1		
-8	**TOP COVER ASSY**	2010208	1		
-9	**BOTTOM COVER**	5210209	1		
-10	**TILT BAIL**	5000055	1		
-11	Foot, Plastic Enclosure	5220003	4		
-12	Line Cord Set - Domestic	5440002	1		
	Line Cord Set - Export	5440017	1		

535/538 MICROWAVE COUNTER continued

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
	PCB ASSEMBLIES			See Page No.	
A100	Counter Interconnect	2020180-01	1	100 - 1	
A101	Power Supply	2020131-01	1	101 - 1	
A105	Microprocessor	2020215-02	1	105 - 1	
A106	Count Chain	2020136-03	1	106 - 1	
A107	Gate Generator	2020197-09	1	107 - 1	
A108	Converter Control (Band 3)	2020200-04	1	108 - 1	
A109	Band 2 Converter	2020139-05	1	109 - 1	
A110	Display and Keyboard Logic	2020140-02	1	110 - 1	
A111	Front Panel Logic	2020191-02	1	111 - 1	
A203	Microwave Converter (535)	2010241-05	1	203 - 1	
	Microwave Converter (538)	2010241-06			
A201A	Voltage Control Oscillator (Not Shown)	2020199-00	1	201A-1	
A201B	IF Amplifier (Not shown)	2020303-01	1	201B-1	
A202	Microwave (YIG) not shown				
	CABLES:				
W7	Front Panel, Flat Ribbon	2040169-01	1		
W19, 20	Front Panel, Harness	2040168-01	1		
W18	Rear Panel, Harness	2040167-01	1		
W10	(A1J111-A109J6) Band 1, Coax	2040165-01	1		
W11	(A112-A109J4) Band 2, Coax	2040166-01	1		
W16	(A108J1-A09J3), Coax	2040208-01	1		
W15	(A106J1-A109J5), Coax	2040210-01	1		
W12, 13	VCO/IF, Harness	2040170-01	1		
W14	(A201BJ1-A106J2), Coax	2040172-01	1		
W9	(A201AJ3-A108J2), Coax	2040174-01	1		
W17	(A201AJ3-A109J1), Coax	2040175-01	1		
W21	Harness Assy	2040227-01	1		
	PROMS:				
A105 –	BASIC PROM SET	2060024-01			
U13	Programmed PROM, Basic 3	6500024-03			
U12	Programmed PROM, Basic 2	6500024-02			
U11	Programmed PROM, Basic 1	6500024-01			
A105 –	GPIB OPTION (2060027-02)				
U16	Programmed PROM, GPIB Option	2060024-01	1	REVISION LEVEL OF PROMS MUST BE SPECIFIED WHEN ORDERING PROM SET	
A105	MATE OPTION				
U19	Programmed PROM, MATE Option	2010636-01		(See label on PROM)	

A100
COUNTER INTERCONNECT
(202180)

FUNCTIONAL
DESCRIPTION
NOT REQUIRED

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A100 COUNTER INTERCONNECT ASSY

2020180 - H

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A100	Counter Interconnect Assy	2020180	1	EIP	34257
J1	Header, Str, 26 pin	2620078	1	3429 - 2302	76381
J2	Header, Str, 50 pin	2620081	2	3433 - 2302	76381
J3	J2				
J4	Friction Lock, 4 pin	2620061	1	09 - 65 - 1049	0000A
J5	Friction Lock, 6 pin	2620090	1	09 - 65 - 1069	"
J6	Header, Str, 7 pin	2620186	1	09-64-1071	"
J7	Header, Str, 10 pin	2620187	1	09-64-1101	"
J8	Friction Lock, 4 pin	2620068	1	640456-4	AMP
XA101	Conn, 11 position	2620183	1	5193-442-1	AMP
XA102	Conn, 50 position	2620185	1	5193-442-3	"
XA103 thru XA109	Conn, 30 position	2620184	7	5193-442-2	"

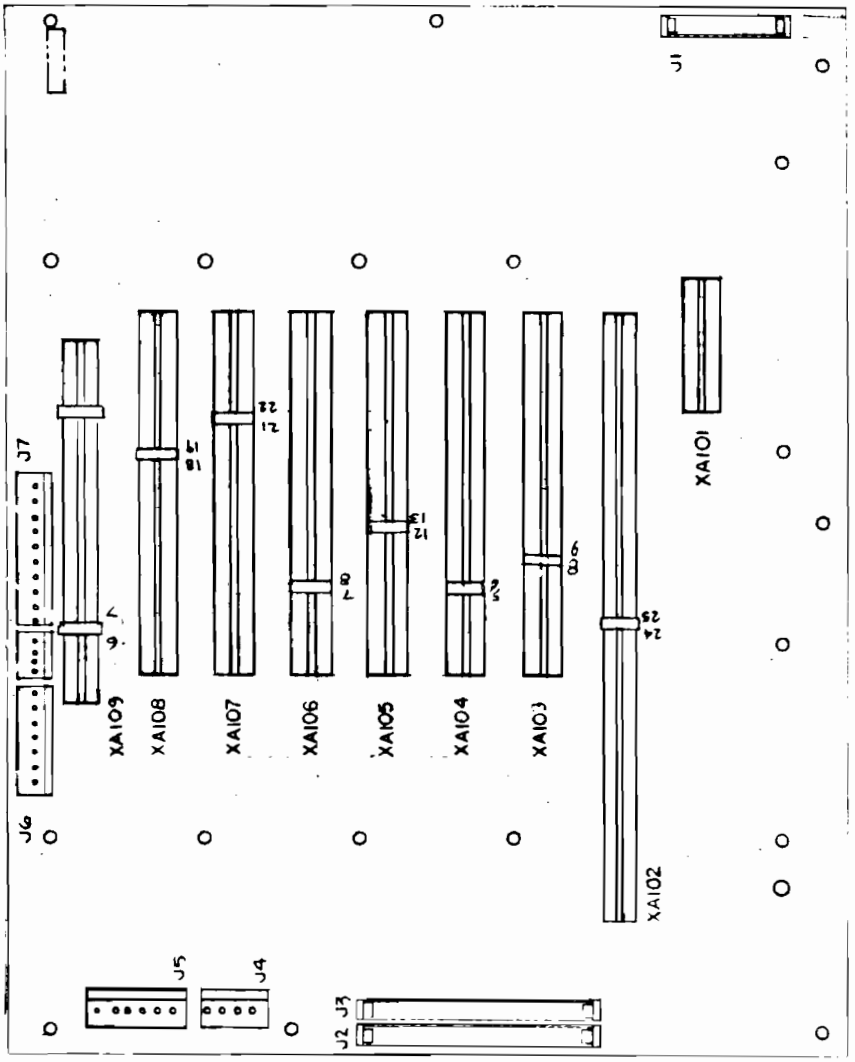

Figure 100-1. Counter Interconnect Component Locator

A101
POWER SUPPLY
(2020131)

The power supply furnishes all basic operating voltages required by the counter. The supply consists of two basic sub-assemblies.

- PC Board (A101), containing the rectifiers, filter capacitors, and regulator circuitry.
- Chassis mounted components consisting of the power transformer (T1); primary wiring; F1 fuse, (100/120V); the 220/240V power programming switch; and the on/off power switch (S101) mounted on the front panel.

The basic voltages required by the counter are unregulated +18V, regulated +5V, −5.2V, +12V and −12V.

The input AC voltage is full wave rectified and filtered to produce DC voltages of ± 9V and ± 18V.

The unregulated +18V is used directly as one supply voltage. The +18V is regulated to a +12V by the action of LM305, a series pass transistor (MJE3055), and foldback current limiting circuitry. The −18V is regulated to a −12V by LM304, a series pass transistor, and foldback current limiting circuitry.

The +9V is regulated to +5V by a three terminal regulator containing thermal and current shutdown circuitry. The −9V current is also regulated to −5.2V by a three terminal regulator that contains thermal and current shutdown circuitry.

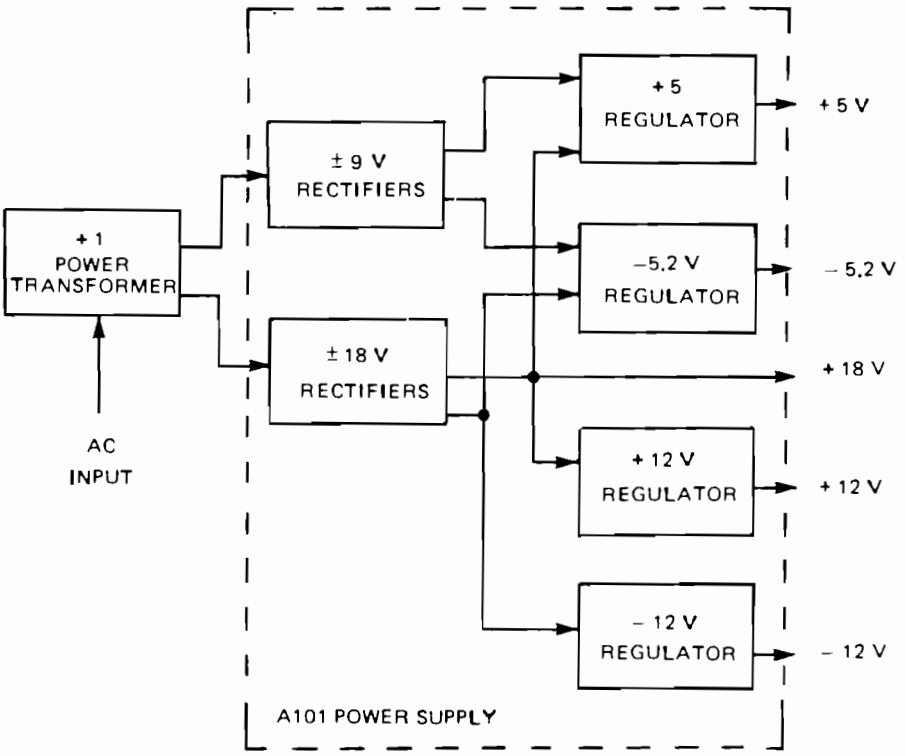

Figure 101-1. Power Supply Block Diagram

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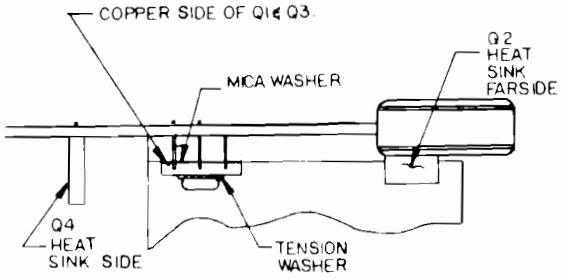
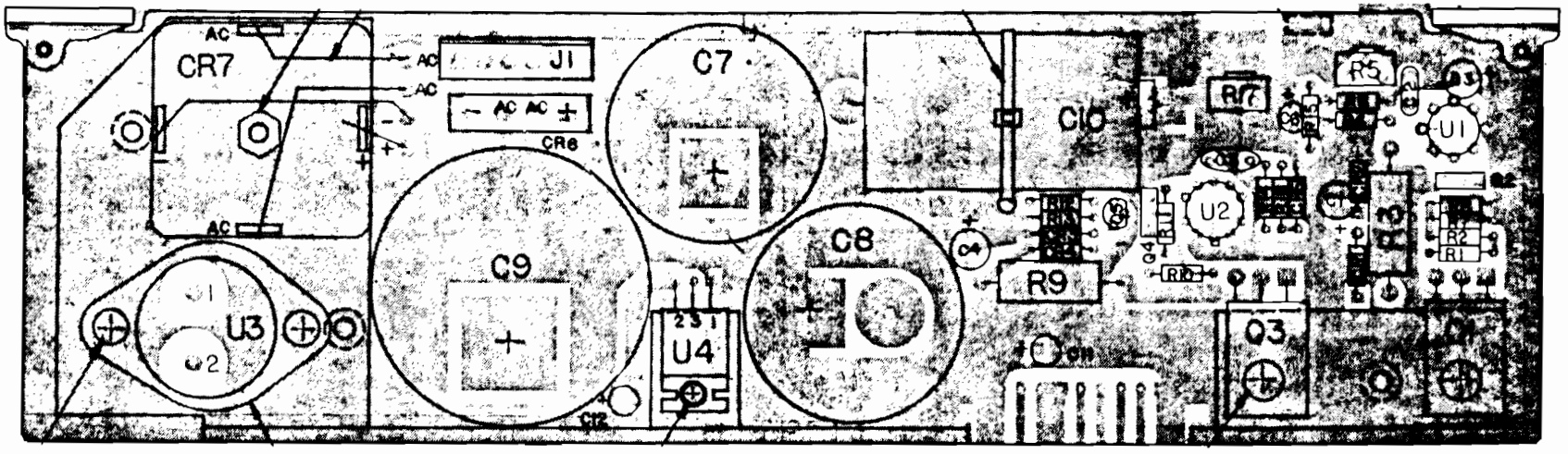
A101 POWER SUPPLY ASSY

2020131-01 L

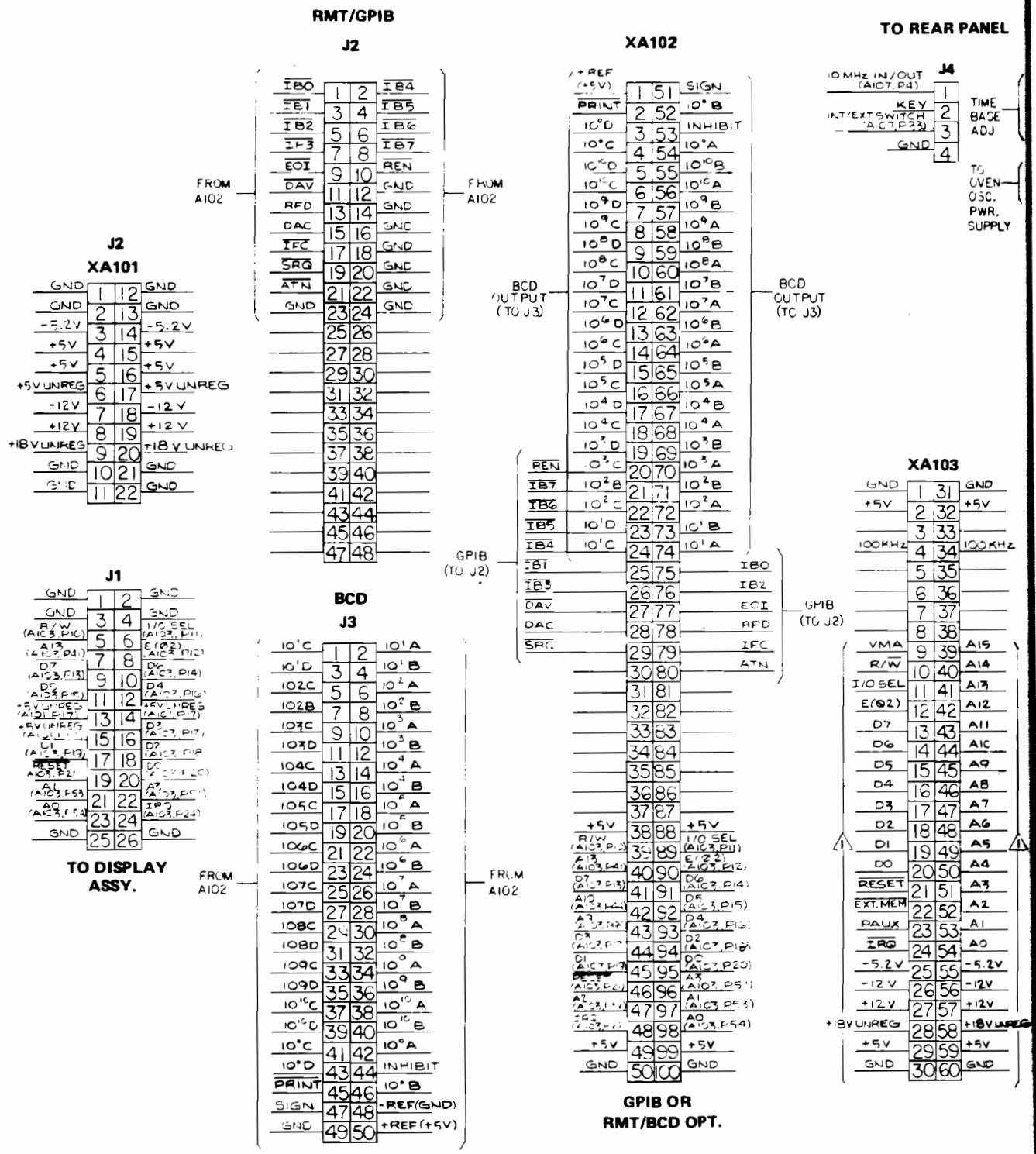
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A101	Power Supply Assy	2020131	1	EIP	34257
C1	Tant, 10μF, 20%, 25V	2300029	3	TAG 20 - 10/25(M)	14433
C2	Mica, 47 pF, 5%, 500V	2260004	1	DM10 - 470J	72136
C3	C1				
C4	Tant, 33μF, 20%, 20V	2300023	1	TAG 20 - 33/20 - 20	14433
C5	Cer, .001μF, 20%, 20V	2150001	1	5GA - D10	56289
C6	Tant, 1.0μF, 20% 35V	2300008	2	TAG 20 -1.0/35 - 50	14433
C7	Elec, 14,000μF, 25V	2200017	1	3110HB143U025	80031
C8	Elec, 9,500μF, 25V	2200016	1	3110HA952U025	80031
C9	Elec, 32,000μF, 15V	2200019	1	3110RB323U015	80031
C10	Elec, 4,900μF, 15V	2200020-00	1	3050JJ4920U15JM	80031
C11	C6				
C12	C1				
CR1 thru CR4	Rectifier	2704001	4	IN4001	07263
CR5	Zener, 12V	2720963	1	IN963A	04713
CR6	Rectifier Brdg	2710029	1	MDA970 - 1	04713
CR7	Rectifier, Brdg	2710028	1	MDA990 - 1	04713
J1	Conn, 6 pin (FRCTN Lock)	2620157	1	640445-6	0000A
Q1	NPN Power	4710001	2	MJE3055	04713
Q2	PNP Power	4710002	2	MJE370	04713
Q3	Q1				
Q4	Q2				
Q5	PNP, General Purpose	4704126	1	2N4126	04713
R1	Comp, 68 ohms, 5%, 1/4 W	4010680	2	RC07GF680J	81349
R2	Met Ox, 36 ohms, 2%, 1/4 W	4130360	1	C4/2%/36	24546
R3	Wire Wound, .66 ohms, 3%, 4W	4110012	2	RS - 2	91637
R4	Prec, 14.7K ohms, 1%, 1/8 W	4061472	1	RN55D1472F	81349
R5	Var. Cer., 500 ohm	4250014	1	72XR500	73138
R6	Prec, 2.26K ohms, 1%, 1/8 W	4062261	1	RN55D2261F	81349
R7	Met Ox, 820 ohms, 2%, 1/4 W	4130821	2	C4/2%/820	24546
R8	R7				
R9	R3				
R10	R1				
R11	Comp, 100 ohms, 5%, 1/4 W	4010101	1	RC07GF101J	81349
R12	Met Ox, 910 ohms, 2%, 1/4 W	4130911	1	C4/2%/910	24546
R13	Met Ox, 12K ohms, 2%, 1/4 W	4130123	1	C4/2%/12K	24546
R14	Prec, 2.43K ohms, 1%, 1/8 W	4062431	1	RN55D2431F	81349
R15	Prec, 4.7K ohms, 2%, 1/4 W	4130472	1	C4/2%/4.7	24546
R16	Met Ox, 1K ohms, 2%, 1/4 W	4130102	1	C4/2%/1K	24546
R17	Var, Cer, 2K ohms	4250016	1	72XR2K	73138
U1	Voltage Regulator	3040305	1	LM305	0000X
U2	Voltage Regulator	3040304	1	LM304	0000X
U3	+5VDC Regulator	3057805-01	1	UA78H05A	07263
U4	-5.2 V Regulator	3057905	1	MC7905.2 CT	04713

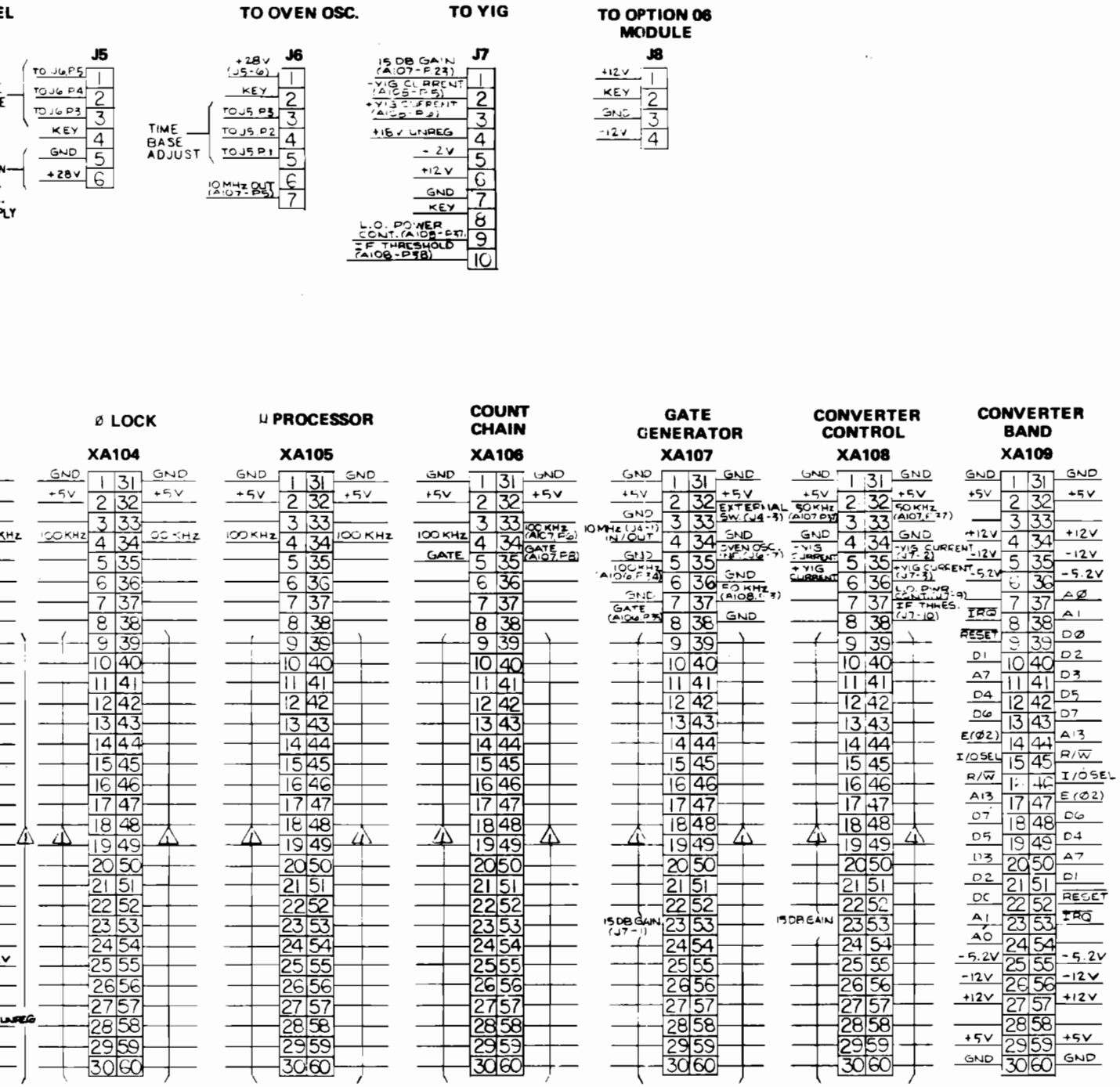




2020131-01-L

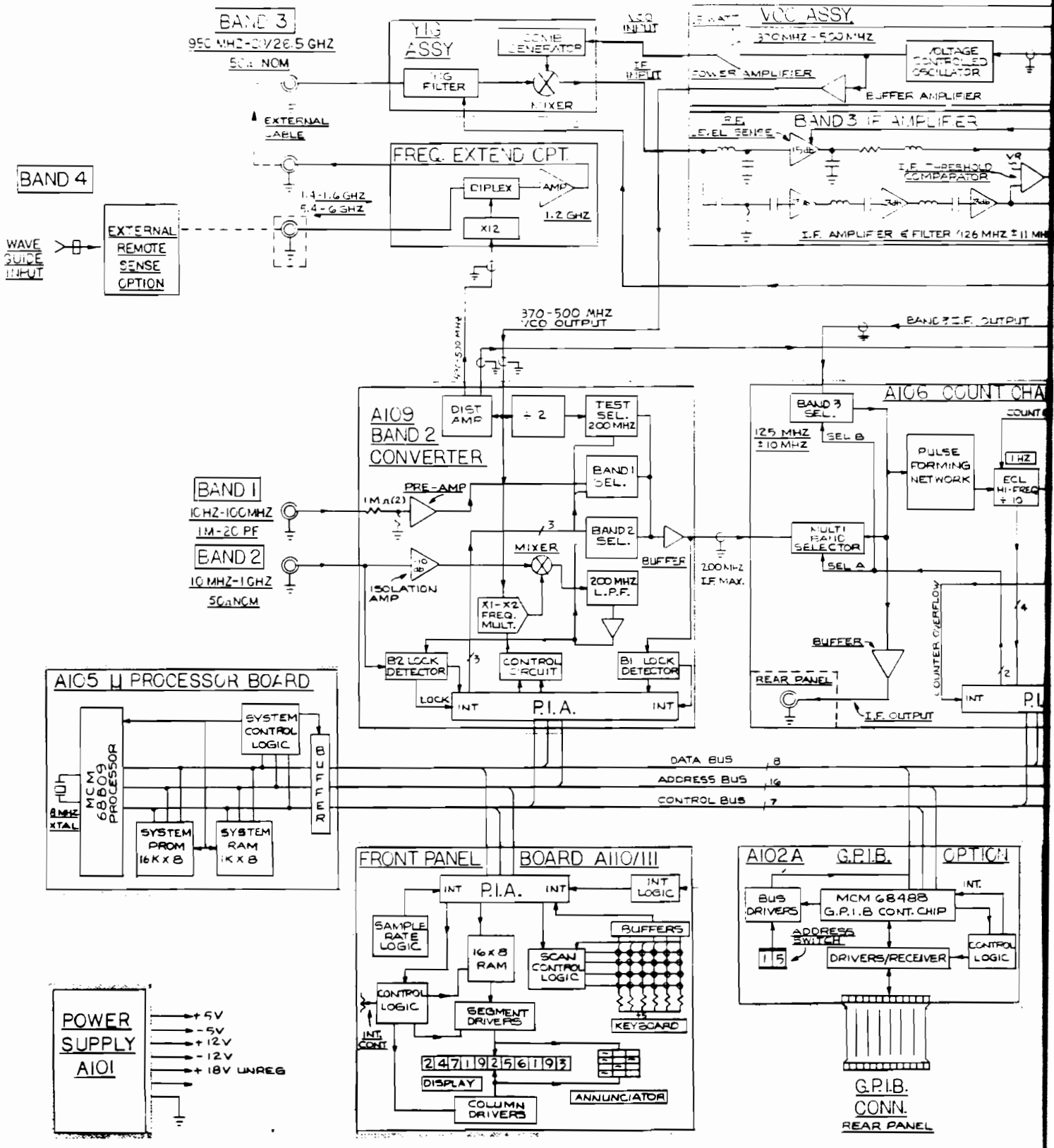
Figure 101-2. Power Supply Component Locator

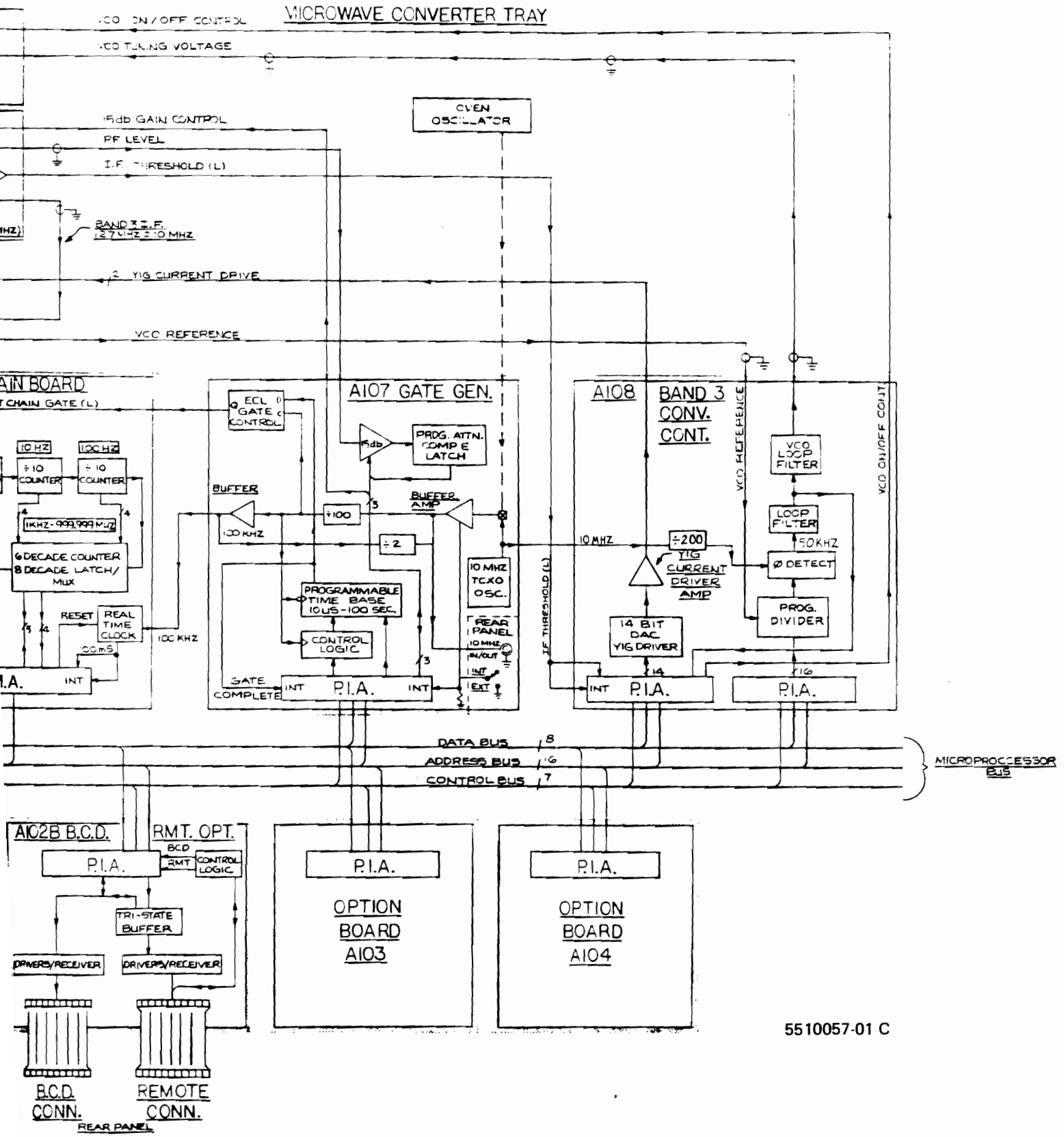

RMT/GPIB
J2
XA102
TO REAR PANEL
J4
10 MHz IN/OUT (A107, P4)
KEY
INT/EXT SWITCH (A107, P33)
GND
TIME BASE ADJ
TO OVEN OSC. PWR. SUPPLY
FROM A102
FROM A102
J2
XA101
BCD OUTPUT (TO J3)
BCD OUTPUT (TO J3)
GPIB (TO J2)
GPIB (TO J2)
XA103
J1
BCD
J3
TO DISPLAY ASSY.
FROM A102
FROM A102
GPIB OR RMT/BCD OPT.
⚠ XA103 THRU XA106 HAVE COMMON CONNECTIONS ON LINES SHOWN IN BRACKETS.



MODIFIED – 5500180-A

Figure 100-2. Counter Interconnect Schematic


BAND 3
950 MHZ-20/26.5 GHZ
50Ω NOM
YIG ASSY
YIG FILTER
COMB GENERATOR
MIXER
ALC INPUT
IF INPUT
VCC ASSY
370 MHZ - 500 MHZ
VOLTAGE CONTROLLED OSCILLATOR
POWER AMPLIFIER
BUFFER AMPLIFIER
EXTERNAL CABLE
FREQ. EXTEND OPT.
DIPLEX
AMP
X12
1.2 GHZ
1.4-1.6 GHZ
5.4-6 GHZ
BAND 4
WAVE GUIDE INPUT
EXTERNAL REMOTE SENSE OPTION
370-500 MHZ VCO OUTPUT
BAND 3 I.F. OUTPUT
A109 BAND 2 CONVERTER
DIST AMP
÷ 2
TEST SEL. 200 MHZ
BAND 1 SEL.
BAND 2 SEL.
PRE-AMP
1MΩ(2)
BAND 1
10 HZ-100 MHZ
1M-20 PF
BAND 2
10 MHZ-1 GHZ
50Ω NOM
ISOLATION AMP
MIXER
BUFFER
200 MHZ L.P.F.
X1-X2 FREQ. MULT.
200 MHZ I.F. MAX.
B2 LOCK DETECTOR
CONTROL CIRCUIT
B1 LOCK DETECTOR
LOCK
INT
P.I.A.
INT
A106 COUNT CHA
BAND 3 SEL.
125 MHZ ±10 MHZ
SEL B
PULSE FORMING NETWORK
1 HZ
ECL HI-FREQ ÷ 10
MULTI BAND SELECTOR
SEL A
BUFFER
REAR PANEL
I.F. OUTPUT
COUNTER OVERFLOW
INT
A105 μ PROCESSOR BOARD
MCM 68809 PROCESSOR
8 MHZ XTAL
SYSTEM CONTROL LOGIC
BUFFER
SYSTEM PROM 16K X 8
SYSTEM RAM 1K X 8
DATA BUS 8
ADDRESS BUS 16
CONTROL BUS 7
FRONT PANEL BOARD A110/111
INT
P.I.A.
INT
INT LOGIC
SAMPLE RATE LOGIC
16 X 8 RAM
SCAN CONTROL LOGIC
BUFFERS
CONTROL LOGIC
SEGMENT DRIVERS
KEYBOARD
INT. CONT
2 4 7 1 9 2 5 6 1 9 3
DISPLAY
ANNUNCIATOR
COLUMN DRIVERS
A102A G.P.I.B. OPTION
INT.
BUS DRIVERS
MCM 68488 G.P.I.B CONT. CHIP
ADDRESS SWITCH
1 5
DRIVERS/RECEIVER
CONTROL LOGIC
G.P.I.B. CONN. REAR PANEL
POWER SUPPLY A101
+5V
-5V
+12V
-12V
+18V UNREG

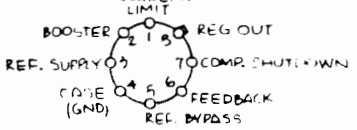


5510057-01 C

Figure 9-1. 535B/538B Block Diagram

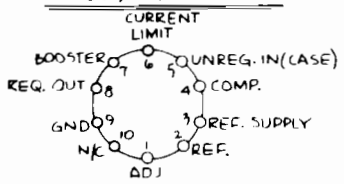
KEY

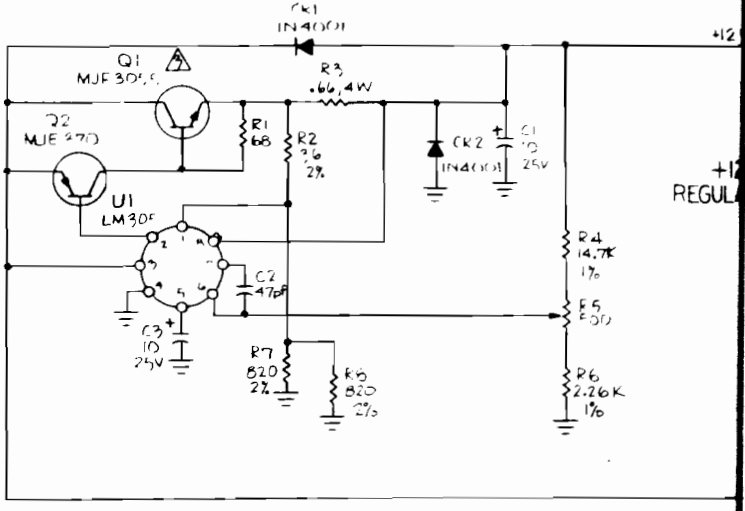
LM305 (U1)

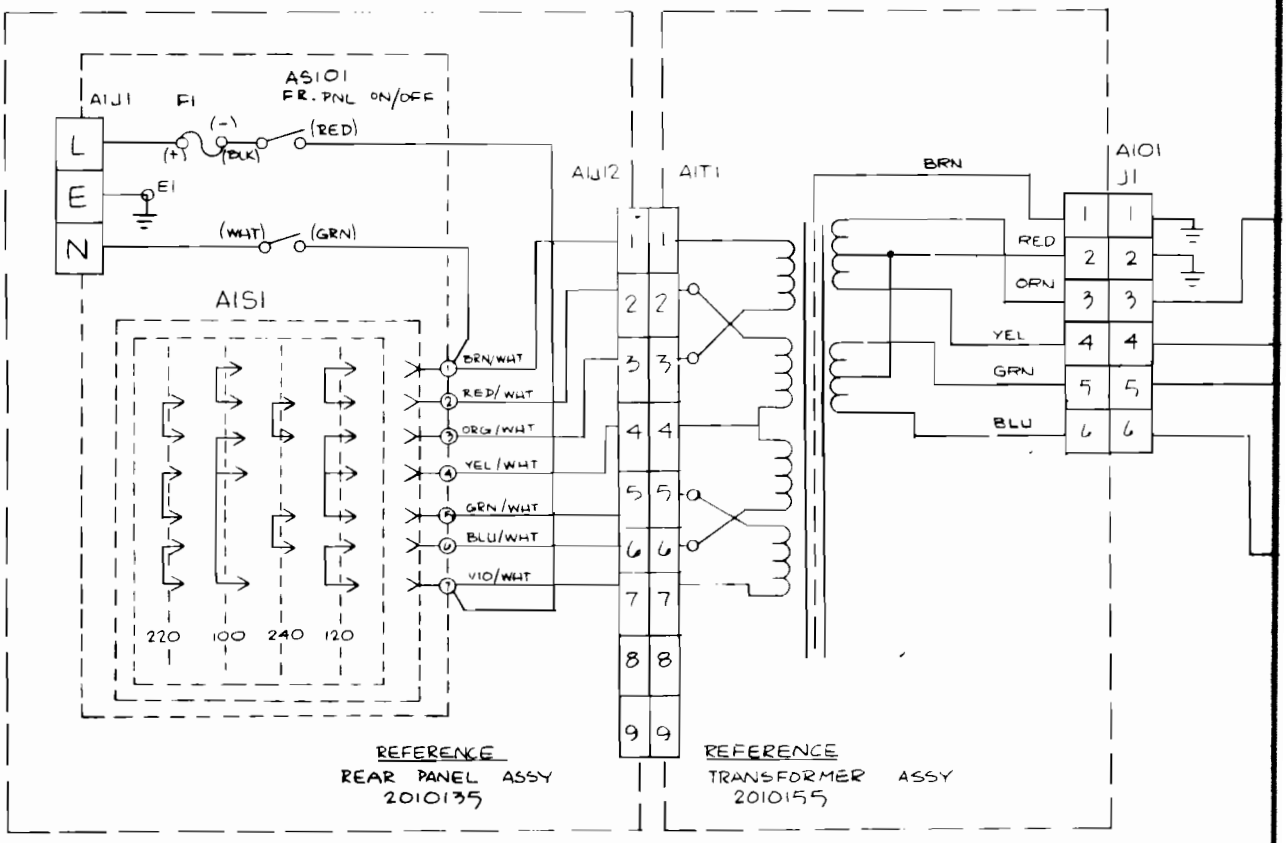


KEY

LM304 (U2)







⚠2 CR7, Q1, Q3, , U3 & U4 ARE MOUNTED ON HEATSINKS.

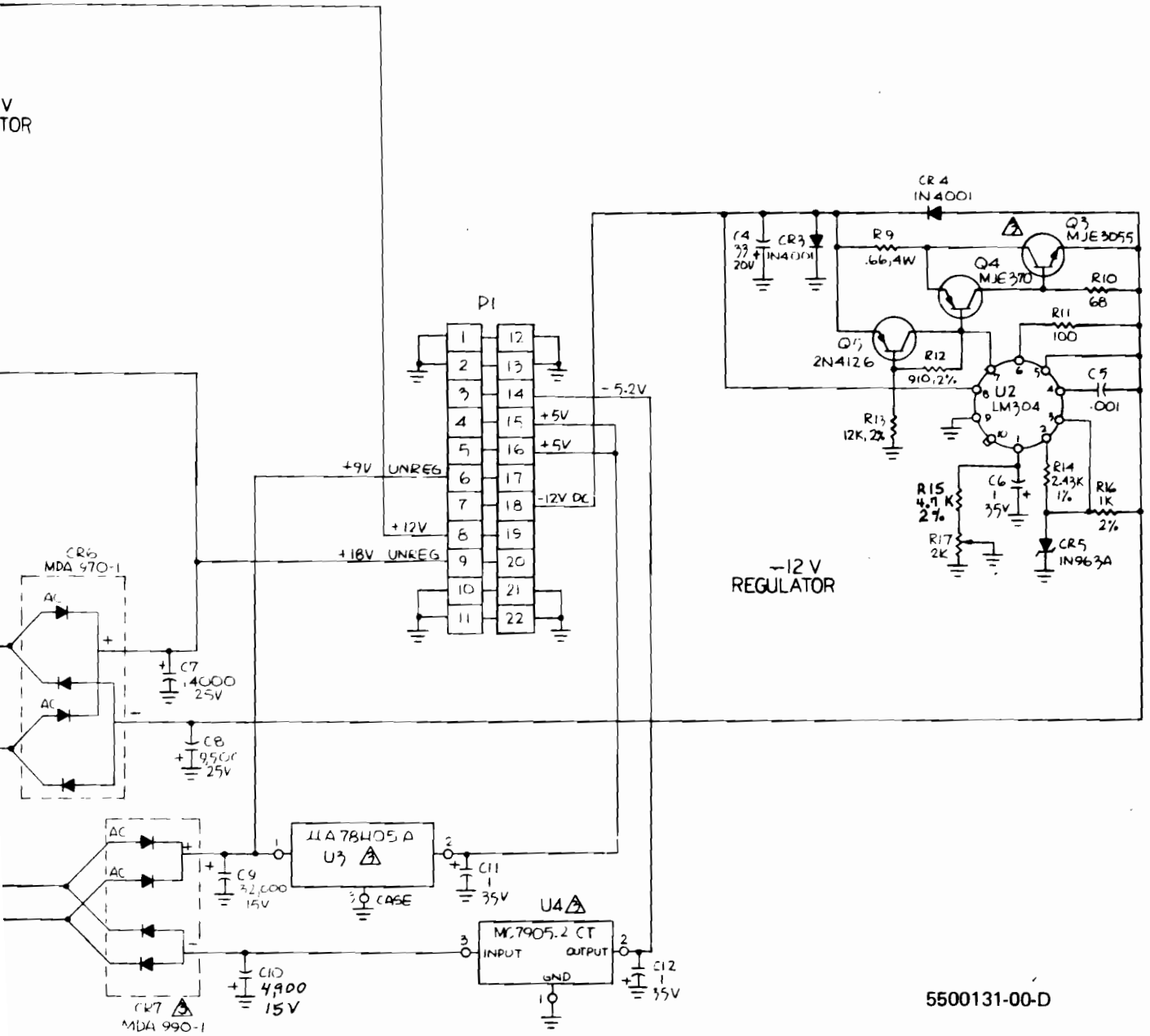


Figure 101-1. Power Supply Schematic

A105
MICROPROCESSOR
(2020215)

The Microprocessor board contains the microprocessor, the control logic, and the firmware for controlling the operation of the counter. The board can be divided into five functional blocks.

1. Microprocessor
2. Power-up reset circuit
3. Address Decoder
4. RAM and Program Memory
5. Control logic and buffers

MICROPROCESSOR

The counter uses a Motorola 68B09 microprocessor. The clock generation circuitry for the digital system is contained within the 68B09. The only external components required for clock generation are two 24-pF capacitor and an AT-cut 8-MHz crystal.

The NMI, FIRO, and DMA functions of the 68B09 are not used. Their corresponding control lines are always disabled. The processor state indicators (BS, BA) are also not used by the counter. The HALT and the MRDY controls are connected to the Interconnect board through the edge connector.

POWER-UP RESET CIRCUIT

The Power-up Reset circuit provides a 100-ms reset signal to the entire digital system after the counter is turned on. The reset signal remains true as long as the +5-volt power supply stays below +4 volts.

When the counter is turned on, the voltage across C5 is 0 volts. The output of the comparator U1 is at logic low. The capacitor C5 slowly charges up through R2. The output of the comparator remains low as long as the voltage across C5 is lower than the voltage on pin 3 of the comparator. When the voltage across C5 becomes higher than that on pin 3, the output of the comparator becomes true, removing the reset signal. R3 is provided for hysteresis purposes. When power is removed, C5 will discharge quickly through CR1.

ADDRESS DECODER

The address decoding is performed by a 4-to-16 line decoder. The 64K-byte address space is divided into sixteen 4K-byte blocks, one of which is always enabled.

The enable signals for the memory blocks become true no later than 51 ns after Q. They stay true until a maximum of 40 ns after E has become false. The 4-to-16-line decoder has open collector outputs. This enables the addressed memory block to be enlarged by wire-ORing two or more outputs together.

The memory map for the counter is as follows:

Volatile RAM Memory	0000 - 07FF
Non-Volatile RAM Memory	0800 - 0FFF
I/O	1000 - 2FFF
Signature Analysis	3000 - 3FFF
Program Memory	4000 - FFEF
Reserved (6809)	FFF0 - FFF1
	FFF2 - FFF3
	FFF4 - FFF5
	FFF6 - FFF7
IRQ	FFF8 - FFF9
	FFFA - FFFB
	FFFC - FFFD
RESET	FFFE - FFFF

RAM AND PROGRAM MEMORY

RAM

A 2K-byte-wide volatile RAM is provided for the normal operation of the counter. To prevent data from being erroneously written into the RAM, the chip enable signal is active only when the E clock and the RAM memory block enable signal from the address decoder are both active and when the A11 address line is at logic 1.

PROM

A block of 48K bytes of memory are assigned for system program. The Microprocessor board contains three 28-pin sockets for PROMs. Each of the sockets is wired to accept a 16K-byte PROM.

CONTROL LOGIC AND BUFFERS

The digital system of the counter contains three buses: the data bus, the address bus, and the control bus.

DATA BUS

The data bus originates from the microprocessor. For signature analysis, the data bus can be disconnected from the rest of the system at the microprocessor by removing jumper header E1. The data bus on the microprocessor board is buffered from the rest of the digital system. The data bus buffer is enabled only when the address space assigned to I/O is addressed. The direction of the data bus buffer is determined by the state of the R/W control line.

ADDRESS BUS

The address bus also originates from the microprocessor. The address bus buffer is always enabled.

CONTROL BUS

The control bus contains eight control lines. Five of the control lines originate from the Microprocessor board. The other three control lines originate from the rest of the digital system.

R/W, E, and Q originate from the microprocessor. Reset is supplied by the power-up reset circuit. The I/O SEL control line is true when A15 and A14 are at logic 0 and either A13 or A12 or both are at logic 1 levels. The IRQ control line is the wired-OR of all the interrupt request lines. MRDY is the wired-OR of the memory ready control lines. The MRDY and HALT control lines are provided for future expansion.

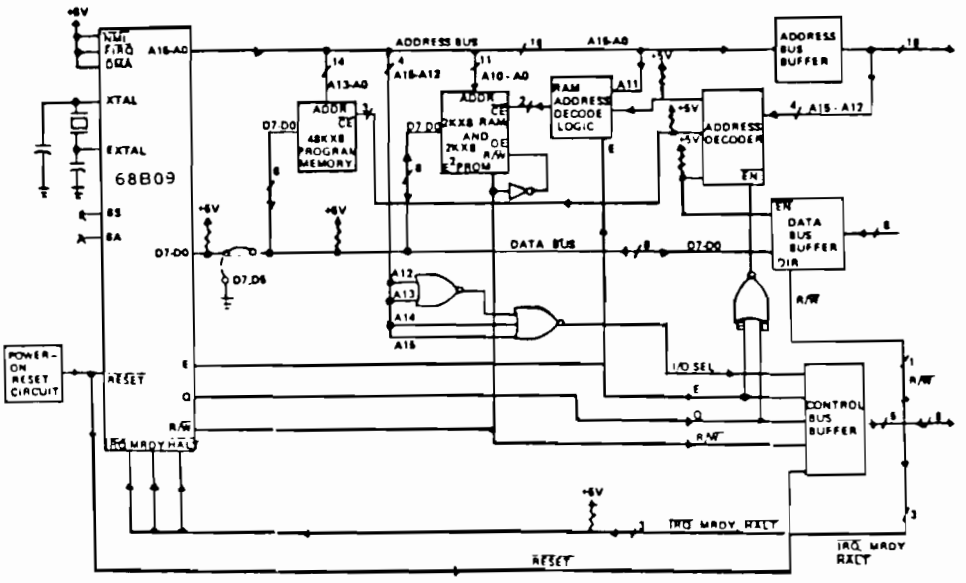


Figure 105-1. Functional Block Diagram, PMicroprocessor

A105 MICROPROCESSOR

2020215-02 A

REF DES	DESCRIPTION	EIP NO.	PER ASSY	TYP MFG NO.	TYP FSCM NO.
C1	Mica, 24pF, 5%, 500V	2260018-00	2	CD10ED240J03	14655
C2	C1				
C3	Disc, 0.01µF, 20%, 100V	2150003-00	14	TG - S10	56289
C4	C3				
C5	Tant, 3.9µF, 10%, 15V	2300027-00	1	196D395X9015HA1	56289
C6	C3				
C7	C3				
C8	C3				
C9	Tant, 33µF, 10V	2300015-00	2	TAPA33M10	14433
C10	C3				
C11	C3				
C12	C3				
C13	C3				
C14	C3				
C15	C3				
C16	C3				
C17	C3				
C18	C3				
C19	C9				
CR1	H/C	2710016-00	1	5082-2835	28480
CR2	ZNR, 3.9V	2705228-01	1	IN5228	04713
R1	Met Ox, IM, 5%, 1/4W	4010105-00	1	RC07GF105J	81349
R2	Met Ox, 22K, 5%, 1/4W	4010223-00	1	RC07GF223J	81349
R3	Met Ox, 300K, 5%, 1/4W	4010304-00	1	RC07GF304J	81349
R4	Not used				
R5	Met Ox, 240, 5%, 1/4W	4010241-00	1	RC07GF241J	81349
R6	Met Ox, 4.7K, 5%, 1/4W	4010472-00	4	RC07GF472J	81349
R7	R6				
R8	R6				
R9	R6				
RN1	Res Ntwrk, 9 x 10k, 2%, 2W	4170003-00	3	782-1-R10K	80740
RN2	RN1				
RN3	RN1				
RN4	Res Ntwrk, 9x4.7k, 2%, 1.25W	4170014-00	1	4310R-101-472	32997
TP1 Thru TP10	Pin, T.P. Swage	2620032-00	10	460-2970-02-03	71279
U1	Int: Volt Comparator	3050311-00	1	MLM311P1	27014
U2	Microprocessor	3050025-00	1	MC68B09	04713
U3	Dvr Hex Bus/Buffer	3084365-00	1	SN74LS365N	01295
U4	Not used				
U5	3 Inp NOR Gate	3087427-00	1	DM74LS27	27014
U6	Dvr Line/Oct Buff Invg	3084244-00	2	SN74LS244N	01295
U7	Not used				
U8	Xcvr Octal Bus	3084245-00	1	SN74LS245N	01295

A105 MICROPROCESSOR

2020215-02 A

REF DES	DESCRIPTION	EIP NO.	PER ASSY	TYP MFG NO.	TYP FSCM NO.
U9	2K x 8 CMOS RAM	3056116-00	1	HM6116LP-4	62786
U10	2K x 8E PROM	6420000-00	1	X2816A	60395
U11	PROM Set: 16K x 8	2060006-00	1		27128
U12	U11				
U13	U11				
U14	3 INP NAND Gate	3087410-00	1	DM74LS10	27014
U15	U6				
U16	4-16 Decoder	3074159-00	1	SN74159N	01295
U17	Hex Inverter	3087404-00	1	DM74LS04	27014
E1	Prog, Header, 16 Pin DIP	5000205-00	1	16-675-191T	51167
Y1	Xtal, 8.00 MHz	2030100-00	1	MP-1	ATRON

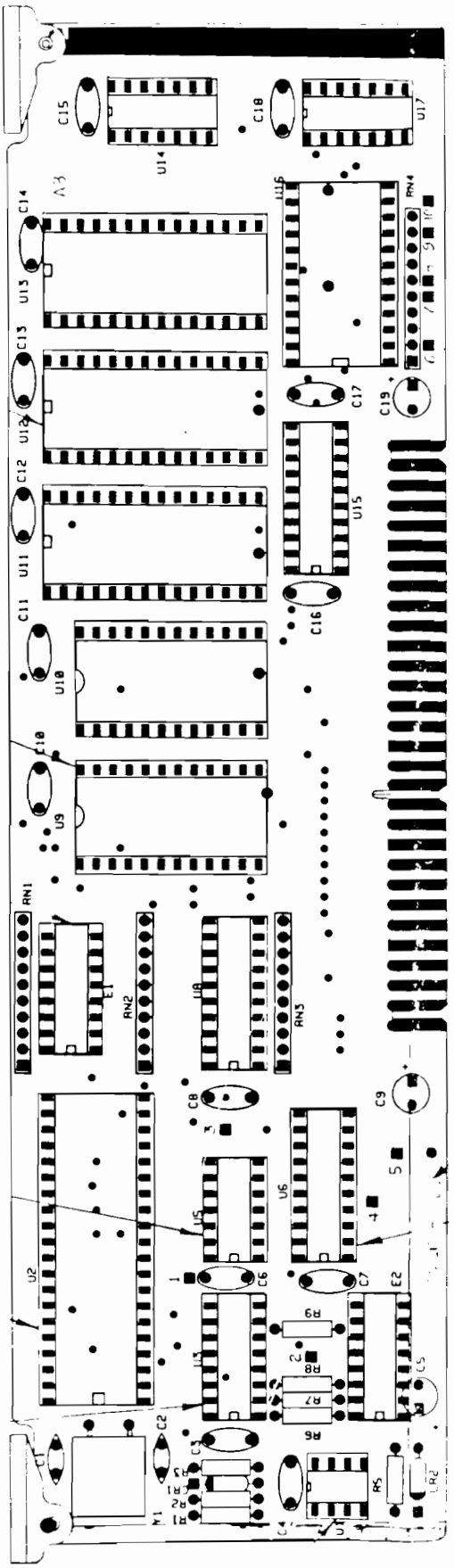
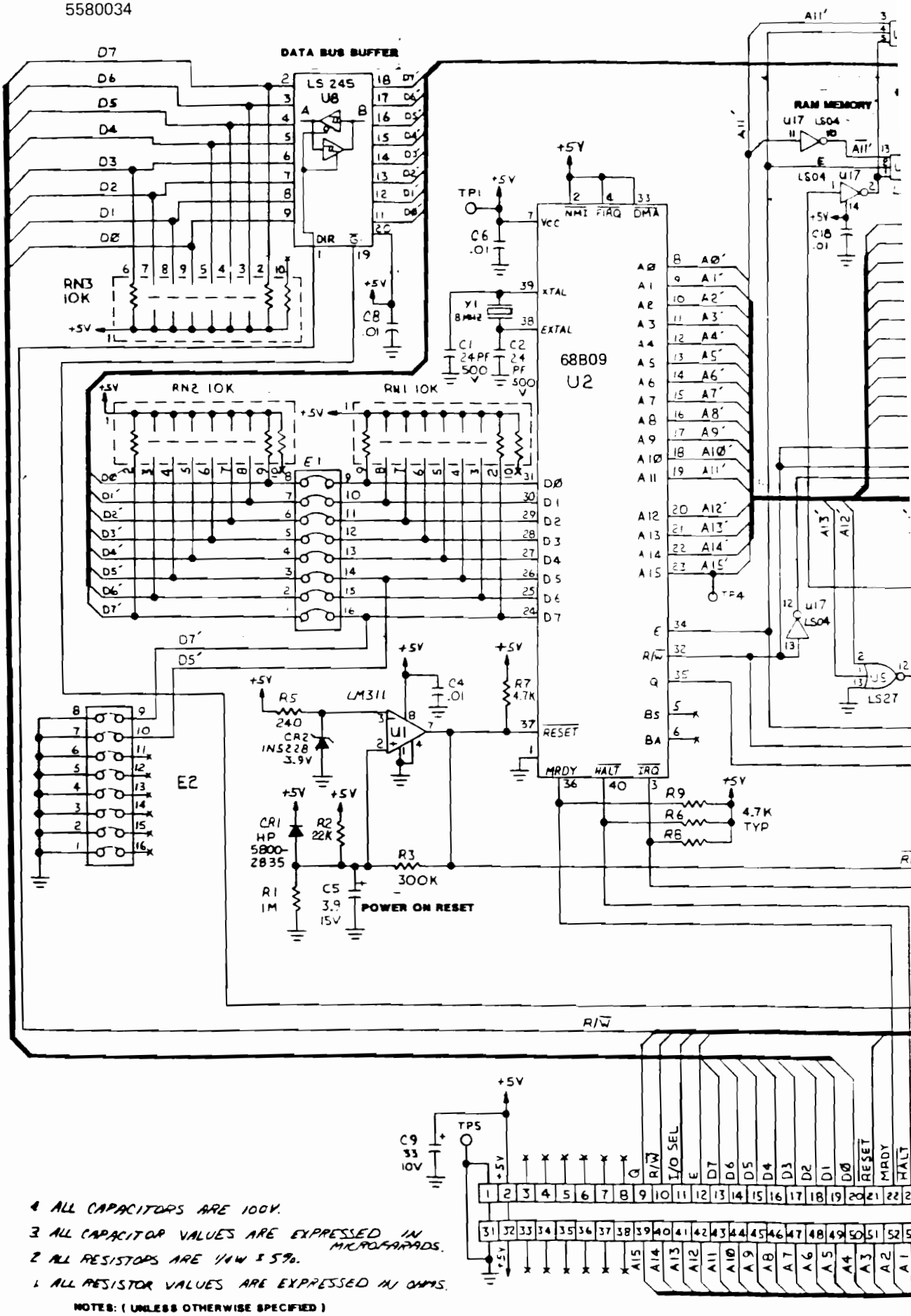


Figure 85-2. Component Locator, Microprocessor

5580034



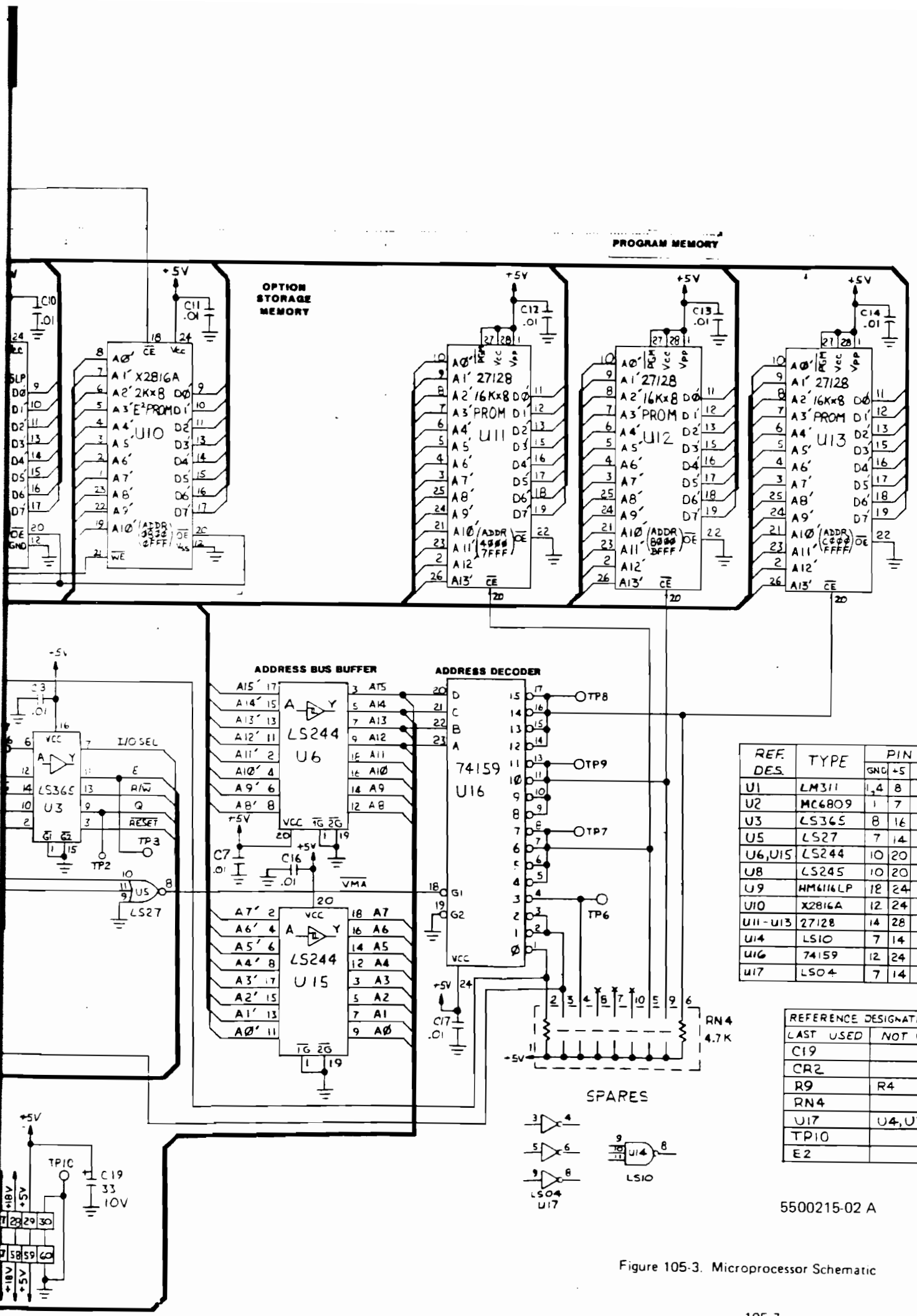
4 ALL CAPACITORS ARE 100V.

3 ALL CAPACITOR VALUES ARE EXPRESSED IN MICROFARADS.

2 ALL RESISTORS ARE 1/4W ± 5%.

1 ALL RESISTOR VALUES ARE EXPRESSED IN OHMS.

NOTES: (UNLESS OTHERWISE SPECIFIED)



REF DES	TYPE	PIN NO. GND	+5		
U1	LM311	1,4	8		
U2	MC6809	1	7		
U3	LS365	8	16		
U5	LS27	7	14		
U6,U15	LS244	10	20		
U8	LS245	10	20		
U9	HM6116LP	12	24		
U10	X2816A	12	24		
U11-U13	27128	14	28		
U14	LS10	7	14		
U16	74159	12	24		
U17	LS04	7	14		

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C19	
CR2	
R9	R4
RN4	
U17	U4,U7,
TP10	
E2	

5500215-02 A

Figure 105-3. Microprocessor Schematic

A106
COUNT CHAIN
(2020136)

The Count Chain Assembly receives IF signals from the Band 3 IF Amplifier (A201B) and the Band 2 Converter (A109). It also receives a gate signal and a 100 kHz reference signal from the Gate Generator (A107). The count chain assembly selects the appropriate IF signal, gates it, and counts it to produce a BCD output that represents the input frequency. It also produces one or two IF output signals to be used for options at J3 and J4.

The A106 board receives two IF input signals on J1 and J2. The appropriate input is selected by enabling one of two differential amplifiers (U1A or U1B). Enabling of the appropriate amplifier is achieved by turning on a transistor switch (Q11 or Q12). The appropriate transistor is turned on by the output of an open collector inverter (U7C or U7A) driven by a TTL signal from the PIA (U10).

The output of the input selector differentially drives a squaring circuit. The squaring circuit consists of a differentially driven current mirror (Q1) driving a tunnel diode (CR5). The voltage across the tunnel diode changes abruptly between two states (approximately 0.2V and 0.5V). The signal across the diode drives the pulse forming circuit. This circuit begins with a high speed differential amplifier (Q2 and Q3). The output of this amplifier drives Q4 which is a current switch. The square wave current, from Q4's collector, drives an inductor (L1). The voltage across the inductor is a series of pulses; a positive pulse when Q4 turns on and a negative pulse when Q4 turns off. Diode CR5 tends to remove the negative pulses and increases the damping to improve the amplitude of the positive pulses. The positive pulses from the generator drive a pulse inverter (Q6). The pulse inverter is a high-speed zero bias amplifier that is biased at cut off by diode CR6.

The output of the pulse inverter (Q6) drives the input to the first decade counter (U2). The bias for the U2 input is established by a tracking bias supply (U3, Q7). The voltage at TP2 is equal to the voltage on U2 pin 1, plus a fixed DC offset selected by R45. The BCD outputs from U2 are slew-rate limited, and can only be seen after the counting ends and comes to rest. The carry output on pin 9 is an ECL level U2 signal, and is always visible.

The ECL output of U2 drives an ECL to TTL converter (Q8, Q9 and Q10). This converter is a differential amplifier with a cascade output buffer (Q8). The response of Q8 is improved by inductive peaking provided by L2. The output of Q8 drives a decade counter (U4) which in turn drives a third decade counter (U5). The BCD outputs of U4 and U5 are connected to a 6 decade counter (U6) which derives its clock information directly from the BCD outputs of U5. When counting is finished, 8 decades of BCD data are read by the microprocessor (through the PIA U10) from U6 by a time multiplex process. The multiplexer (set to the first digit by the end of the previous reset clock) loads the multiplex latches with the $\overline{\text{Latch Load}}$ clock, and steps to the remaining 7 digits with 7 pulses on the $\overline{\text{Scan Clock}}$ line. The first decade of BCD data from U2 is read directly from the PIA.

A single reset line is used to reset all count stages to zero before the next count cycle begins.

A real-time clock (U8, U9) is also on the count chain assembly. This circuit takes the 100kHz reference signal that is coming from the Counter Interconnect Assembly (A100), and divides it by 10,000 to give a 10Hz (100ms) clock. The output from this clock is fed to the PIA to allow the microprocessor to gather time information at a 10Hz rate for timing functions within the program.

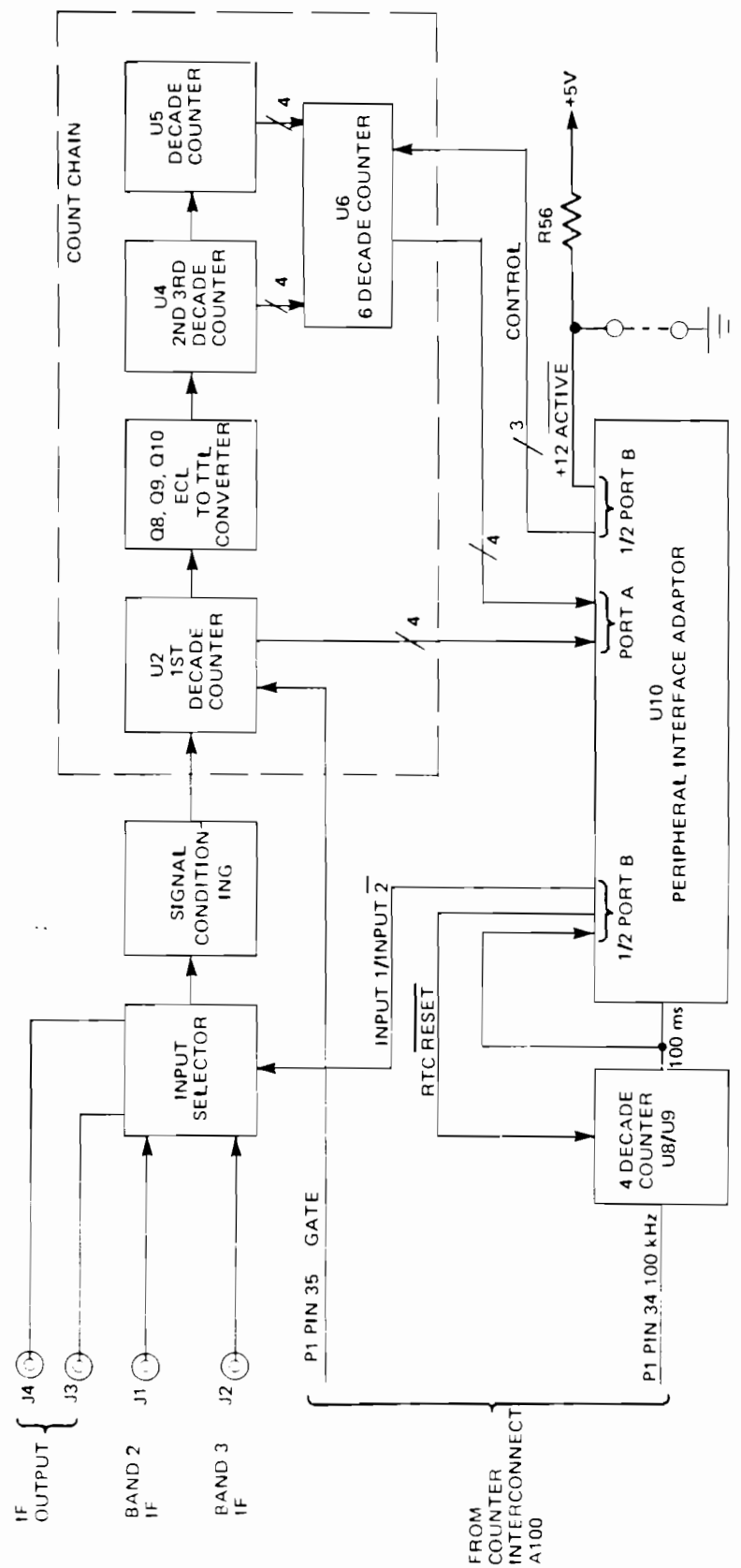


Figure 106-1. Count Chain Block Diagram

A106 COUNT CHAIN ASSY

2020136-03 C

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A106	Count Chain Assy	2020136	1	EIP	34257
C1	Tant, 33μF, 20%, 10V	2300015	5	TAG 20 - 33/10 - 50	14433
C2	Cer., .01μF, 20%, 100V	2150003-00	17	TG - S10	56289
C3	C2				
C4	C1				
C5	Mica, 10pF, 5%, 500V	2260012	1	CD100J03	72136
C6	Tant, 10μF, 20%, 25V	2300029	4	DF106M259	72136
C7	C2				
C8	C2				
C9	Cer., .001μF, 20%, 1KV	2150001	3	5GA - D10	56289
C10	C2				
C11	Not used				
C12	C9				
C13	C2				
C14	C6				
C15	C6				
C16	C2				
C17	C9				
C18	Not Used				
C19	Not Used				
C20	C1				
C21	C2				
C22	C1				
C23	Not Used				
C24 thru C28	C2				
C29	C1				
C30 thru C33	C2				
C34	C6				
CR1	General Purpose	2704148-00	3	IN4148	07263
CR2	Zener, 6.2V	2705234	1	IN5234	04713
CR3	CR1				
CR4	Tunnel, Switching	2710033	1	G00010C	20754
CR5	Hot Carrier	2710004-00	1	5082 - 2835	28480
CR6	CR1				
L1	Part of Board				
L2	Inductor, 1μH	3510003	1	DD 1.0	72259
Q1	PNP, RF	4704959	1	2N4959	04713
Q2	NPN, Microwave	4710032	3	NE02137	18324
Q3	Q2				
Q4	PNP, RF	4710010	1	MPS - H81	04713
Q5	PND, RF GRADED	4710013	1	2N5179	34257
Q6	NPN, RF	4710026	1	NE73432B	0000S
Q7	Q2				
Q8	NPN, RF	4705179	3	2N5179	04713
Q9	Q8				
Q10	Q8				
Q11	PNP, General Purpose	4704126	2	2N4126	04713
Q12	Q11				

A106 COUNT CHAIN ASSY, continued

2020136-03 C

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R1	Comp., 1.5K, 5%, 1/4 W	4010152	2	RC07GF152J	81349
R2	Comp., 6.2K, 5%, 1/4 W	4010622	2	RC07GF622J	81349
R3	Comp., 51 ohm, 2%, 1/4 W	4130510-00	2	C4/2%/51	24546
R4	Comp., 5.1K, 5%, 1/4 W	4010512	2	RC07GF512J	81349
R5	Comp., 2.7K, 5%, 1/4 W	4010272	2	RC07GF272J	81349
R6	Comp., 51 ohm, 5%, 1/4 W	4010510	1	RC07GF510J	81349
R7	Met Ox, 2K, 2%, 1/4 W	4130202	3	C4/2%/2K	24546
R8	Comp., 510 ohm, 5%, 1/4 W	4010511	1	RC07GF511J	81349
R9	Comp., 5.6 ohm, 5%, 1/4 W	4010569	5	RC07GF5R6J	81349
R10	R5				
R11	R9				
R12	Met Ox, 68 ohm, 2%, 1/4 W	4130680	1	C4/2%/68	24546
R13	Met Ox, 43 ohm, 2%, 1/4 W	4130430	1	C4/2%/43	24546
R14	Met Ox, 3.9K, 2%, 1/4 W	4130392	1	C4/2%/3.9K	24546
R15	R7				
R16	R4				
R17	R1				
R18	R2				
R19	Comp., 100 ohm, 5%, 1/4W	4010101	1	RC07GF101J	81349
R20	Met Ox, 56 ohm, 2%, 1/4 W	4130560	2	C4/2%/56	24546
R21	R9				
R22	R20				
R23	Comp., 200 ohm, 2%, 1/4 W	4130201	4	RL07S201G	24546
R24	R9				
R25	Met Ox, S.A.T. (2K, 2% Nom)	4130999	1	C4/2%/XX	24546
R26	Met Ox, 39 ohm, 2%, 1/4 W	4130390	2	C4/2%/39	24546
R27	R23				
R28	Met Ox, 270 ohm, 2%, 1/4 W	4130271	1	C4/2%/270	24546
R29	R3				
R30	Not used				
R31	Comp, 10 ohm, 5%, 1/4 W	4010100	1	RC07GF100J	81349
R32	Met Ox, 47 ohm, 2%, 1/4 W	4130470	1	C4/2%/47	24546
R33	Met Ox, 20 ohm, 2%, 1/4 W	4130200	1	C4/2%/20	24546
R34	Met Ox, 510 ohm, 2%, 1/3 W	4130511	1	C4/2%/510	24546
R35	R9				
R36	Met Ox, 1K, 2%, 1/4 W	4130102	3	C4/2%/1K	24546
R37	R26				
R38	Comp., 390 ohm, 5%, 1/4 W	4010391	1	RC07GF391J	81349
R39 thru R42	Comp, 10 K, 5%, 1/4 W	4010103	4	RC07GF103J	81349
R43	Met Ox, 20 K, 2%, 1/4 W	4130203	4	C4/2%/20K	24546
R44	R43				
R45	R36				
R46	R43				
R47	Met Ox, 18 ohm, 2%, 1/4 W (NOM) SAT	4130999	1	C4/2%/18	24546
R48	R43				
R49	Met Ox, 240 ohm, 2%, 1/4 W	4130241	1	C4/2%/240	24546
R50	R23				
R51	R23				
R52	R36				
R53	Met Ox, 430 ohm, 2%, 1/4W	4130431	1	C4/2%/430	24546

A106 COUNT CHAIN ASSY, continued

2020136-03 C

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R54	R7				
R55	Comp., 1.8K, 5%, 1/4 W	4010182	1	RC07GF182J	81349
R56	Comp., 4.7K 5%, 1/4 W	4010472	1	RC07GF472J	81349
TP1 thru TP10	Conn., Pin, .040D	2620032	10	460-2970-0203	71279
U1	Dual/Diff Ampl	3043049	1	CA3049T	07263
U2 Alt.	High Spd. Div.	3018636	Ref.	SP8636D	
U2	UHF, BCD, Decade Counter	3010637	1	SP8637B	58317
U3	Op Amplifier	3040741	1	UA741CP	27014
U4	PST Decade Counter	3084196	1	SN74LS196N	01295
U5	4 Bit Decade Counter	3084160	1	SN74LS160N	01295
U6	6 Dec. Ctr/8 Dec. Latch	3057031	1	LS74031	01295
U7	Hex Inverter	3087404	1	SN74LS04N	04713
U8	Decade Counter	3084490	2	74LS490N	01295
U9	U8				
U10	Periph. Interface Adapter	3086821	1	MC68B21P	04713

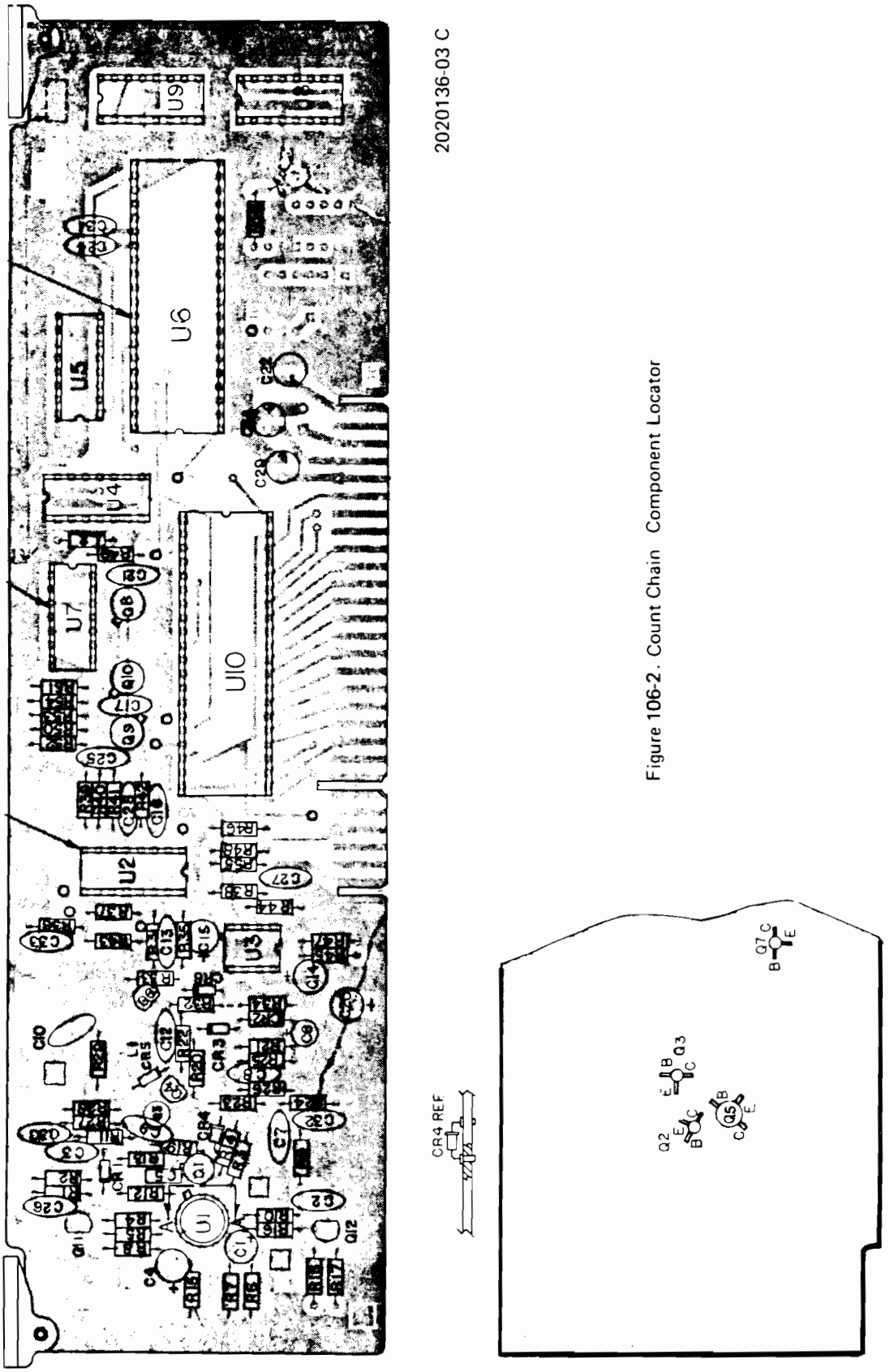
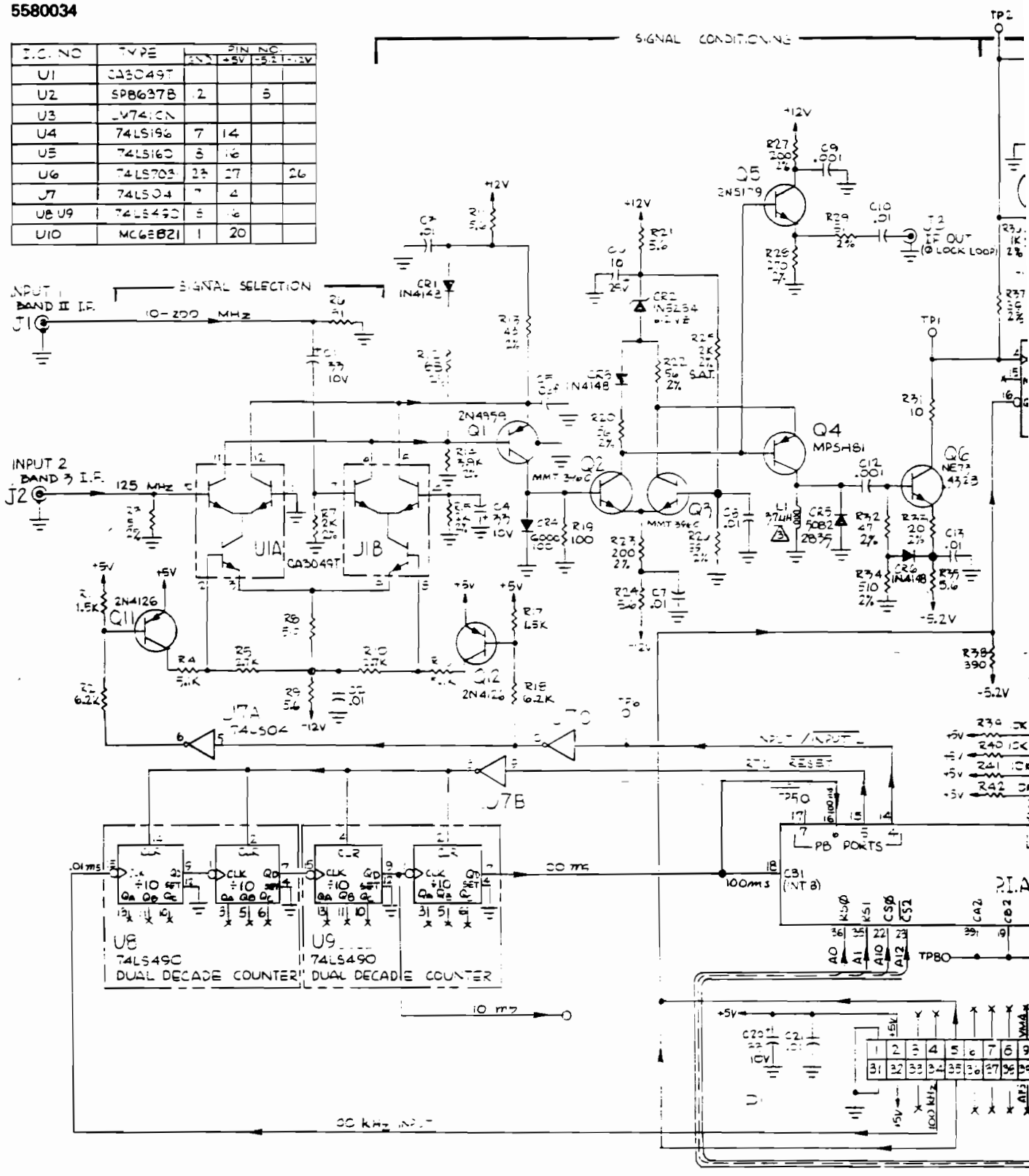


Figure 106-2. Count Chain Component Locator

I.C. NO	TYPE	PIN NO.			
		GND	+5V	-5.2	-12V
U1	CA3049T				
U2	SPB637B	2		5	
U3	LM741CN				
U4	74LS196	7	14		
U5	74LS160	8	16		
U6	74LS703	23	27		26
U7	74LS04	7	4		
U8 U9	74LS490	5	10		
U10	MC6821	1	20		

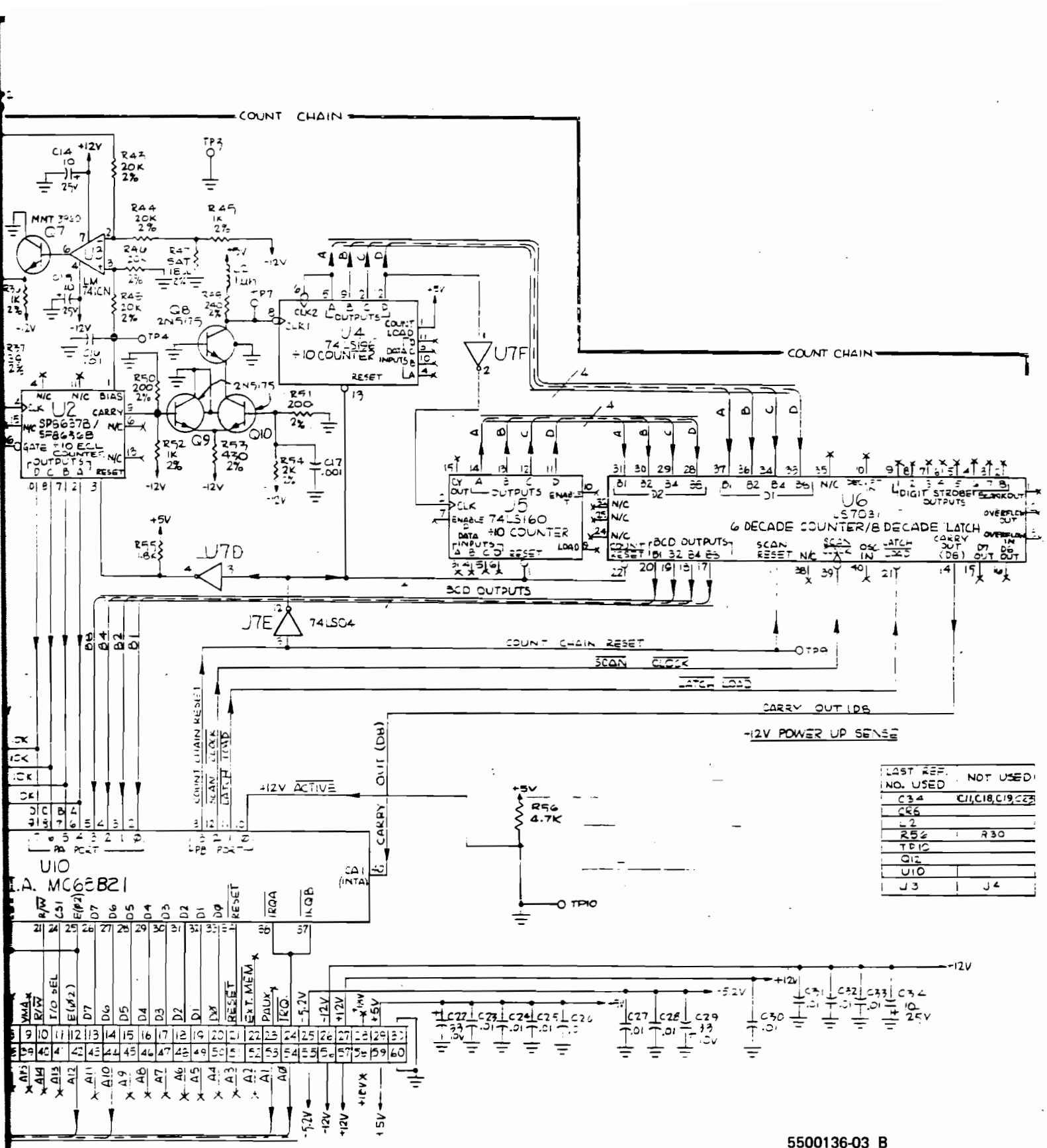


⚠3 INDUCTOR PART OF P.C. BOARD.

2 ALL CAPACITOR VALUES ARE EXPRESSED IN MICROFARADS.

1 ALL RESISTORS ARE ¼W 5%. RESISTANCE IS EXPRESSED IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED



LAST REF. NO. USED	NOT USED
C34	C11,C18,C19,C22
CR6	
L2	
R56	R30
TP10	
Q12	
U10	
J3	J4

5500136-03 B

Figure 106-3. Count Chain Schematic

A107
GATE GENERATOR
(2020197)

This assembly performs the following functions.

- Reference Oscillator Control
- Gate Generation
- Band 3 Amplitude Determination

REFERENCE OSCILLATOR CONTROL

This circuit selects, as the time base for the counter, either the internal reference oscillator or an external 10 MHz signal applied to the rear panel. This circuit provides a 100 kHz TTL level clock signal for the gate generator, a 10 MHz TTL level clock signal for the microwave converter and, in the internal oscillator mode, a 10 MHz signal (1 volt p-p into 50 ohms) to the rear panel

The 10 MHz internal reference signal is applied to a switchable "analog to TTL" converter (Q1, Q2, Q3). When the Ref Int Ext line is high the TTL converter is enabled. One output goes to drive Q4, giving a square wave (1V p p into 50 ohms) on the 10 MHz Ref line. A second output goes to NAND gate U1 (also switchable for signal isolation) The output of U1 goes to J3 to be used by the microwave converter. The output of U1 also goes to the clock input of U2. U2 is a dual decade divider that divides by 100. The output of U2 is a 100 kHz TTL clock signal to the gate generator.

When the Reference Int/Ext line is set to external (low) the TTL converter (Q1, Q2, Q3) and driver (Q4) are disabled, TTL converter (Q5, Q6, Q7) is enabled, and U1 is set to select the external input. An external reference signal applied to the 10 MHz reference line is then converted to the input of U2

GATE GENERATOR

The Gate Generator must provide an accurate, stable, signal gate to the Count Chain. The gate must be switchable, in decade increments, between 100 microseconds and 1 second. The gate generator consists of a programmable divide-by-N time base (U5), a dual flip-flop (U6A, U6B), and an ECL flip flop (U8). The divide ratio of U5, which determines the gate time, is set by U5 pins 12, 13, and 14 as follows.

Pin 12	Pin 13	Pin 14	Divide Ratio	Gate Time
0	0	1	10^1	100 μsec
0	1	0	10^2	1 Msec
0	1	1	10^3	10 Msec
1	0	0	10^4	100 Msec
1	0	1	10^5	1 sec

The outputs of U5 and U6 enable ECL flip-flop U8, but U8 is clocked directly from the 100kHz clock to insure gate accuracy.

When the gate is not active, U5 is permitted to free-run by holding U6B clear (T0). The gate is initialized by setting U6B. This clears U6A and clears U5 (T1). The next clock pulse sets U8 (T2). The gate is then enabled by momentarily clearing U6B (T3). The next clock sets U6A which enables U5 and U8 (T4). At T5 the gate is opened and U5 begins counting clocks (T5). Halfway through the gate, U5 pin 1 goes high (T6). After U5 has accumulated the proper number of clocks its output, pin 1, goes low. This sets U6B, which clears U6A, and sets U8 pin 7 high (T7). The next clock closes the gate (T8). The program next clears U6B (T9), which enables the gate to free-run again (T0). See figure 107-1.

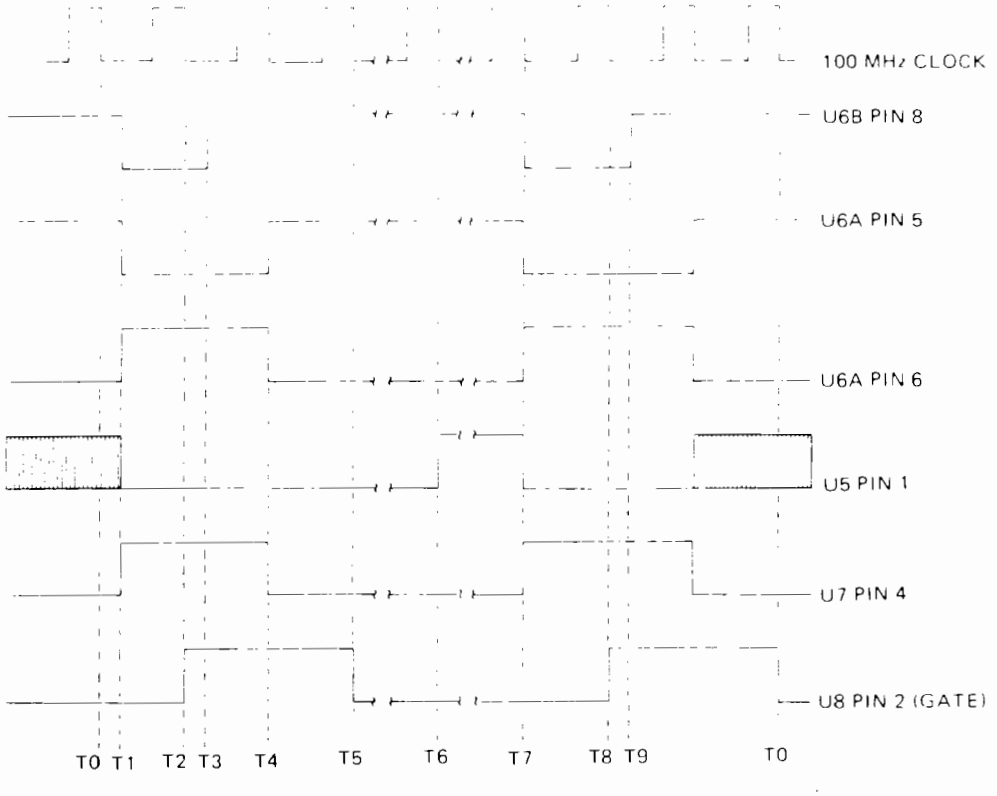


Figure 107-1. Gate Generator Timing Diagram

BAND 3 AMPLITUDE DETERMINATION

This circuit consists of three main parts.

- THE POWER METER ZERO DAC is used to automatically zero offsets in the Power Meter. It consists of two 8 bit latching DACs (U3, U4), and a comparator (U14A). All the latching DACs are driven in parallel by shift register U16, with the appropriate DAC being written to by the four write lines (U15, pins 2, 4, 6, 8). The coarse DAC (U3) has a range of ± 200 micro amps, and the fine DAC (U4) has a range of +1.5 micro amps. The Power Meter Zero DAC (U3) is adjusted so that on step 1 U14A is not set, but on the next step U14A is set. This adjusts the input to U14 to 0 volts, nulling any offsets in the power meter circuit.

- THE POWER METER consists of a 15 dB switchable gain stage (U9), an 8 bit DAC used as a variable attenuator (U10), a 100 mV comparator (U14B), and a latch (half of U17). Two variable attenuators are used, on counters equipped with the option 02 power meter, to provide greater resolution (U10, U12).

  When the detected signal from the microwave converter enters U9 the power meter is first set for maximum gain and minimum attenuation. Next the latch (U17) is reset. If the input to the comparator (U14B) is greater than 100 mV, latch U17 will be set. The signal amplitude to the comparator is then reduced, and the process is repeated until latch U17 no longer gets set. The input amplitude can then be calculated from the switch and DAC settings. The amplitude is calculated to a 3 dB resolution.

PERIPHERIAL INTERFACE ADAPTER (PIA)

The Peripherial Interface Adapter (U18) is used as the microprocessor I/O port. It has an address range from 9900 Hex to 9903 Hex. Peripheral Port A is at address 9900, and Peripheral Port B is at address 9902.

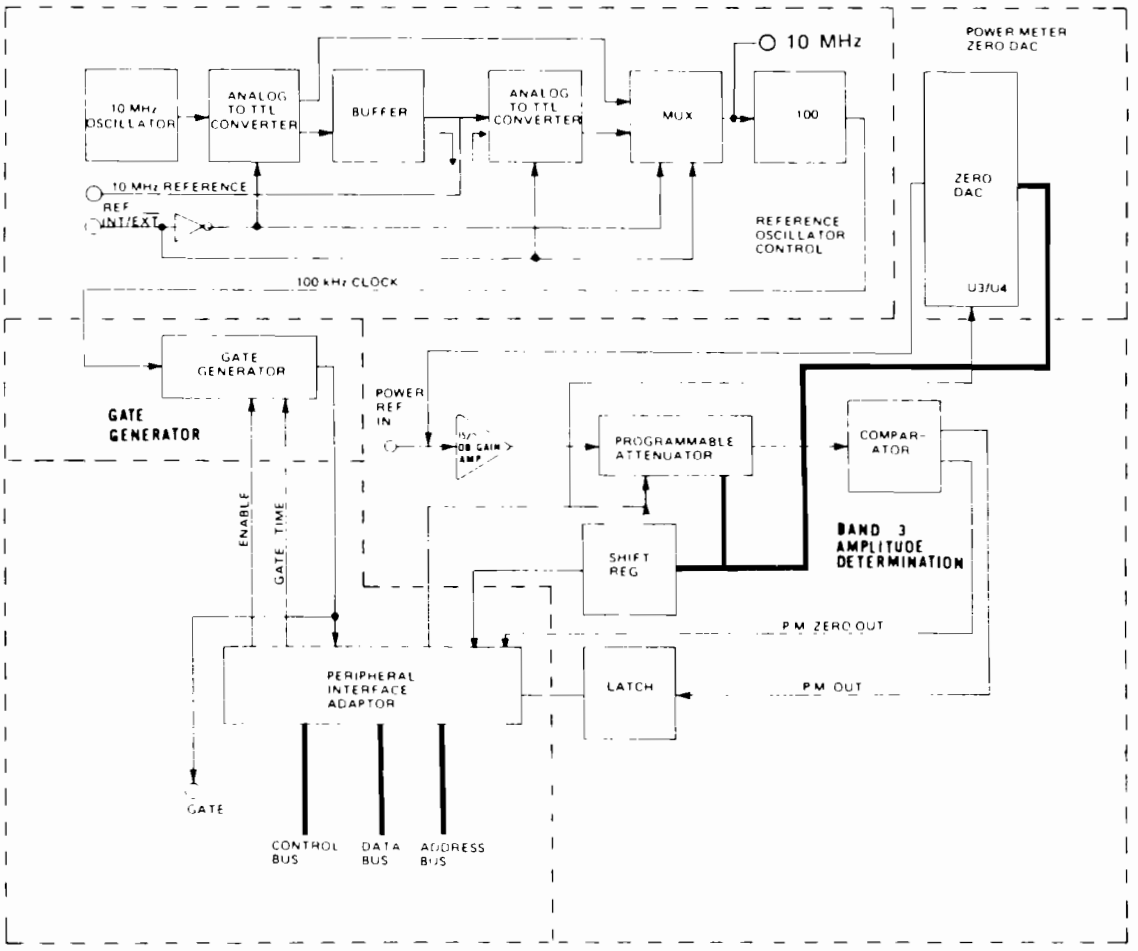


Figure 107-2. Gate Generator Block Diagram

A107 GATE GENERATOR

2020197-09,10 B

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A107	Gate Generator Assy 05/06	2020197	1	EIP	34257
	A113 Crystal Osc	2030002	Ref		
C1	Cer, .01μF, 20%, 100V	2150003	15	TG-S10	72982
C2	C1				
C3	Tant, 33μF, 20%, 10V	2300015	4	TAPA33M10	14433
C4 thru C7	C1				
C8	Mica, 22pF, SAT	2269999	1	CD10ED220J03	72136
C9	Tant, 1μF, 20%, 35V	2300008	1	TAPA 1.0M35	14433
C10	Mica, 33pF, 5%, 500V	2260021	2	CD10ED330J03	72136
C11	Mica, 100pF, 5%, 500V	2260034	1	CD10FD101J03	72136
C12	C10				
C13 thru C15	C1				
C16	Tant, 10μF, 20%, 25V	2300029	2	DF106M25S	NEC
C17	C1				
C18	C3				
C19	C3				
C20	C1				
C21	C1				
C22	C3				
C23	C1				
C24	C1				
C25	C16				
C26	C1				
CR1	Hot Carrier	2710004	1	FH1100	07263
CR2	Hot Carrier	2710006	1	5002-2800	HP
CR3	CR1 - Option only				
CR4	Zener, 6.2V	2700827	1	IN827	
R1	Comp, 10 ohm, 5%, 1/4W	4010100	2	RC07GF100J	81349
R2	Comp, 1K, 5%, 1/4W	4010102	2	RC07GF102J	81349
R3	Comp, 620, 5%, 1/4W	4010621	2	RC07GF621J	81349
R4	Comp, 2.2K, 5%, 1/4W	4010222	3	RC07GF222J	81349
R5	Comp, 220, 5%, 1/4W	4010221	2	RC07GF221J	81349
R6	Comp, 510, 5%, 1/4W	4010511	2	RC07GF511J	81349
R7	Comp, 200, 5%, 1/4W	4010201	1	RC07GF201J	81349
R8	Comp, 27, 5%, 1/4W	4010270	1	RC07GF270J	81349
R9	Comp, 300, 5%, 1/4W	4010301	1	RC07GF301J	81349
R10	Comp, 4.7K, 5%, 1/4W	4010472	6	RC07GF472J	81349
R11	R1				
R12	Comp, 2K, 5%, 1/4 W	4010202	2	RC07GF202	81349
R13	R10				
R14	R4				
R15	R5				
R16	R6				
R17	R3				
R18	Met Ox, 5.6K, 2%, 1/4W	4130562	1	C4/2%/5.6K	24546
R19	Met Ox, 3.3K, 2%, 1/4W	4130332	1	C4/2%/3.3K	24546
R20	Met Ox, 27, 2%, 1/4W	4130270	1	04/1%/27	24546
R21	Comp, 2.7K, 5%, 1/4W	4010272	1	RC07GF272J	81349
R22	R10				
R23	R10				
R24	R2				

A107 GATE GENERATOR continued

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R25	R12				
R26	R4				
R27	Met Ox, 30K, 2%, 1/4W	4130303	1	C4/2%/30K	24546
R28	Met Ox, 39K, 2%, 1/4W	4130393	1	C4/2%/39K	24546
R29	Prec, 1.69K, 1%, 1/10W	4051691	1	RN55C1691F	81349
R30	Prec, 1.82K, 1%, 1/10W	4051821	1	RN55C1821F	81349
R31	Prec, 57.6K, 1%, 1/10W	4055762	1	RN55C5762F	81349
R32	Comp, 36K, 5%, 1/4W	4010363	1	RC07GF363F	81349
R33	Comp, 15K, 5%, 1/4W	4010153	1	RC07GF153F	81349
R34	Met Ox, 750, 2%, 1/4W	4130751	1	C4/2%/750	24546
R35	Prec, 6.19K, 1%, 1/8W	4056191	1	RN55C6191F	81349
R36	Prec, 100, 1%, 1/8W	4051000	1	RN55C1000F	81349
R37	R10				
R38	R10				
R39	Met Ox, 10K, 2%, 1/4W	4130103	2	C4/02/10K	24546
R40	R39				
*R41	Comp, 10K, 5%, 1/4W (option only)	4010103	1	RC07GF103J	81349
RN1	Network, 6.8K	4170005	1	764-1-R6.8K	80740
Q1	NPN - General Purpose	4704124	4	2N4124	
Q2	PNP - General Purpose	4704126	3	2N4126	
Q3	Q1				
Q4	Q2				
Q5	Q1				
Q6	Q2				
Q7	Q1				
Q8	DMOS, FET SW	4710031	1	SD215	18324
U1	Quad NAND	3084132	1	SN4LS132	01295
U2	Dual Decade Counter	3084490	1	SN74LS490N	01295
U3	8 Bit DAC	3057524	3	AD7524JN	
U4	U3				
U5	Digital P Chan. MOS Divider	3035009	1	MK5009P	
U6	D Type Pos Flip-flop	3087474	2	SN74LS74N	01295
U7	Quad 21NP NOR Gate	3087402	1	SN74LS02N	01295
U8	Digital Dual D Flip-flop	3110131	1	MC10131L	04713
U9	Dual Low Noise Op Amp	3045534	1	NE5534N	
U10	8 Bit DAC Buff	3057524	2	AD7524LN	
U11	Op Amplifier Buff	3040308	2	LM308AN	27014
U12	U10 (Option 02 only)				
U13	U11				
U14	Comparator , Dual Low Pwr/volt	3050393	1	LM393N	27014
U15	Hex Buffer/Driver	3007407	1	DM7407N	27014
U16	Dual 4 Bit Static S/R	3034015	1	MC14015B	04713
U17	U6				
U18	Periph. to MC6800	3086821	1	68B21P	04713
U19	Oct, Buffers	3084244		SN74LS244	18324
U20	PROM Set	2060002-03		6400002-04	27014
U21	6 Bit Bus	3078136		DM8136	34257
U22	Quad Dual Flip-flop	3084175	1	SN74LS175	01295
U23	Op Amp/Lin	3040741	1	LM741CN	27014
TP14	PC, Pin 0.40D	2620032	4	466-2976-02-03	71279

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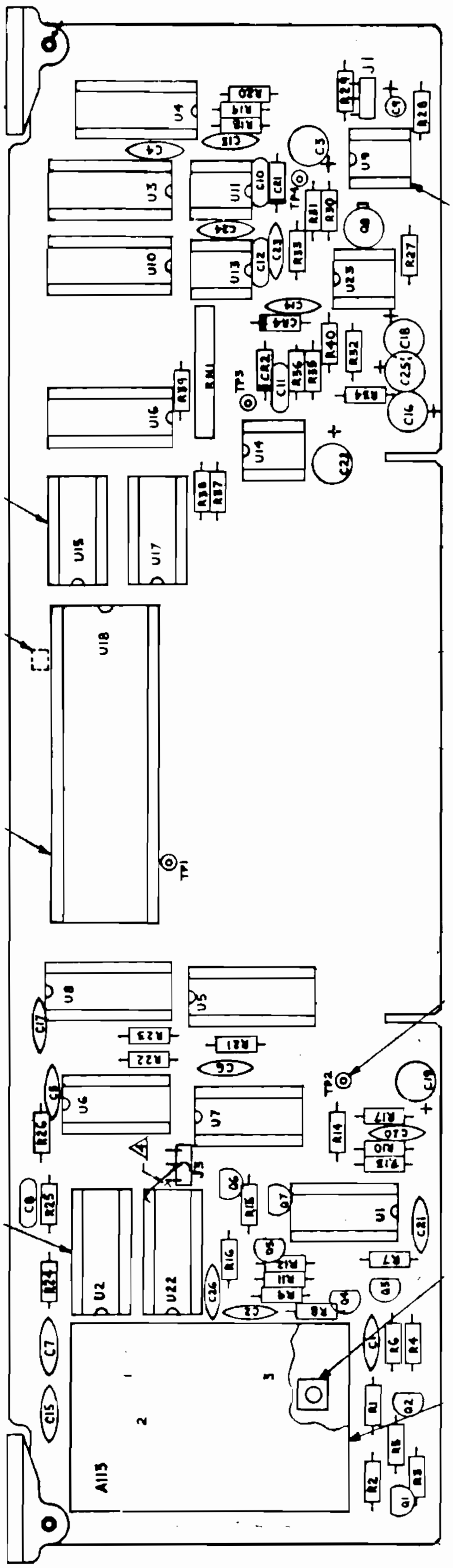
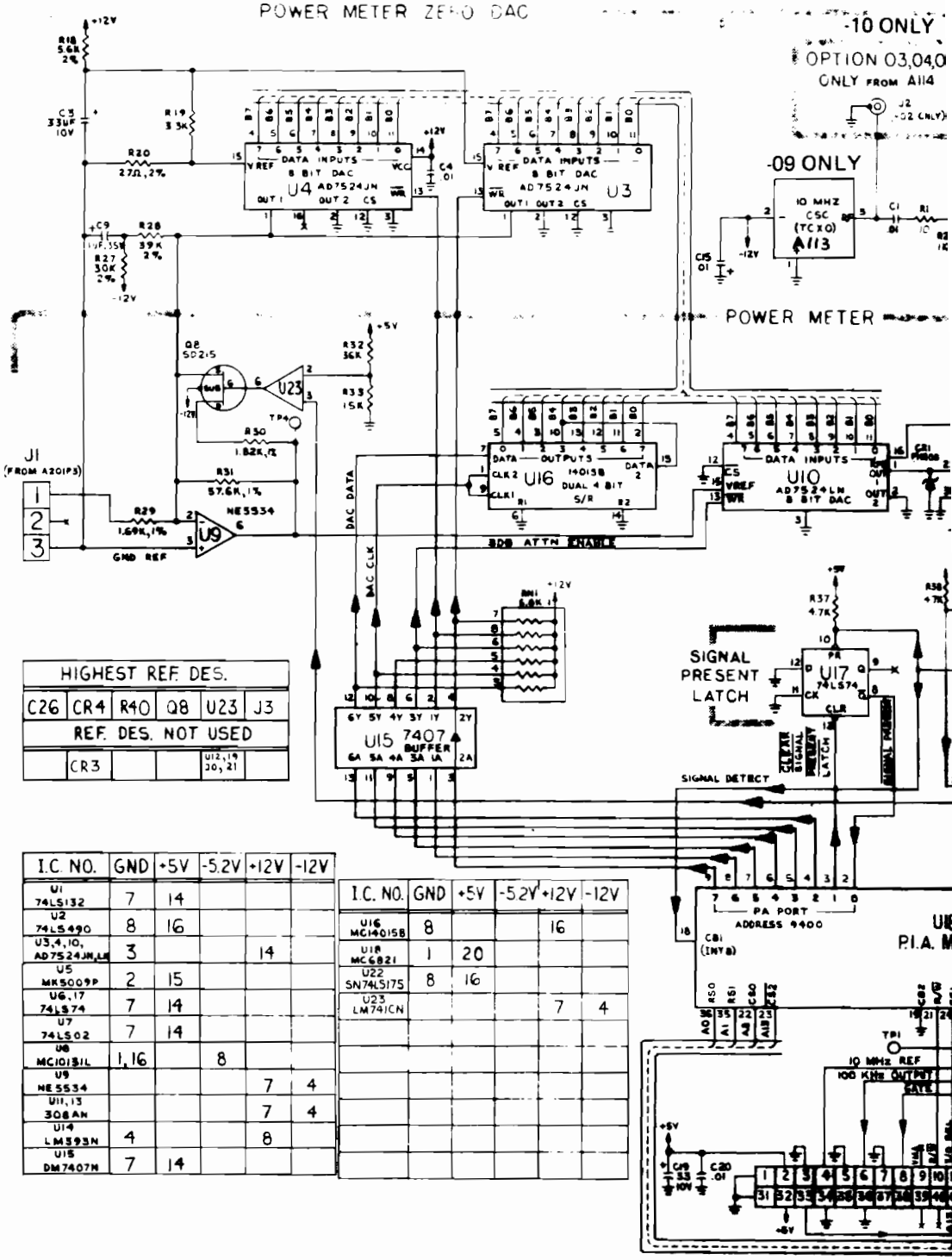


2020197-09,10 B

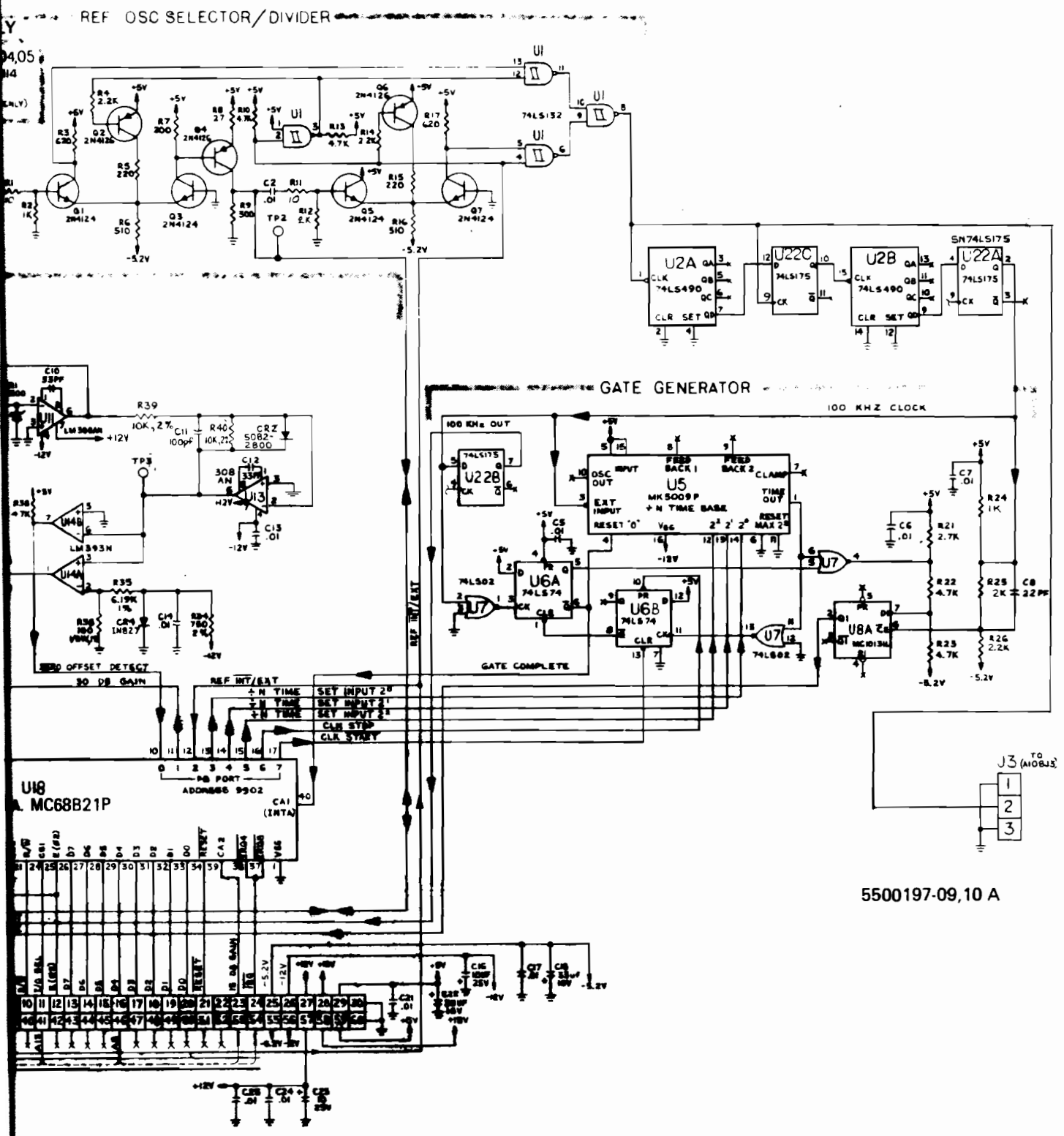
Figure 107-3. Gate Generator Component Locator



HIGHEST REF. DES.					
C26	CR4	R40	Q8	U23	J3
REF. DES. NOT USED					
	CR3			U12,19 20, 21	

I.C. NO.	GND	+5V	-5.2V	+12V	-12V
U1 74LS132	7	14			
U2 74LS490	8	16			
U3,4,10, AD7524JN,LN	3			14	
U5 MK5009P	2	15			
U6,17 74LS74	7	14			
U7 74LS02	7	14			
U8 MC1013IL	1,16		8		
U9 NE5534				7	4
U11,13 308AN				7	4
U14 LM393N	4			8	
U15 DM7407N	7	14			

I.C. NO.	GND	+5V	-5.2V	+12V	-12V
U16 MC14015B	8			16	
U18 MC6821	1	20			
U22 SN74LS175	8	16			
U23 LM741CN				7	4



5500197-09,10 A

Figure 107-4. Gate Generator Schematic

A108
CONVERTER CONTROL
(2020200)

The Converter Control performs two major functions. One of the functions is to provide a precise YIG tuning current which is controlled by the microprocessor via P.I.A. U4. The other function is to phase lock the VCO in the microwave converter to a selected harmonic of a 50 kHz reference signal to provide a synthesized L.O. The converter control also permits the microprocessor to control the L.O. power amplifier and provides the microprocessor input for the I. F. threshold signal.

YIG FREQUENCY CONTROL DAC and DRIVERS

The YIG tuning current is supplied by the YIG driver (U3, Q1, Q2, & Q3) which is controlled by the DAC. The DAC is composed of a 12 bit monolithic DAC (U2), summing amplifier (U1) and resistors to provide a total resolution of 14 bits. PA ports 0 and 1 of the P.I.A. (U4) are used to drive the 2 least significant bits of the DAC directly. A change is the least significant bit of the DAC corresponds to a YIG frequency change of 2 MHz. A voltage analog of YIG current appears across R25 and is compared to the DAC output at the summing junction of U3, with resistors R1 and R19.

The slope of YIG current vs DAC voltage is adjustable with R6 and the offset is adjusted with R10.

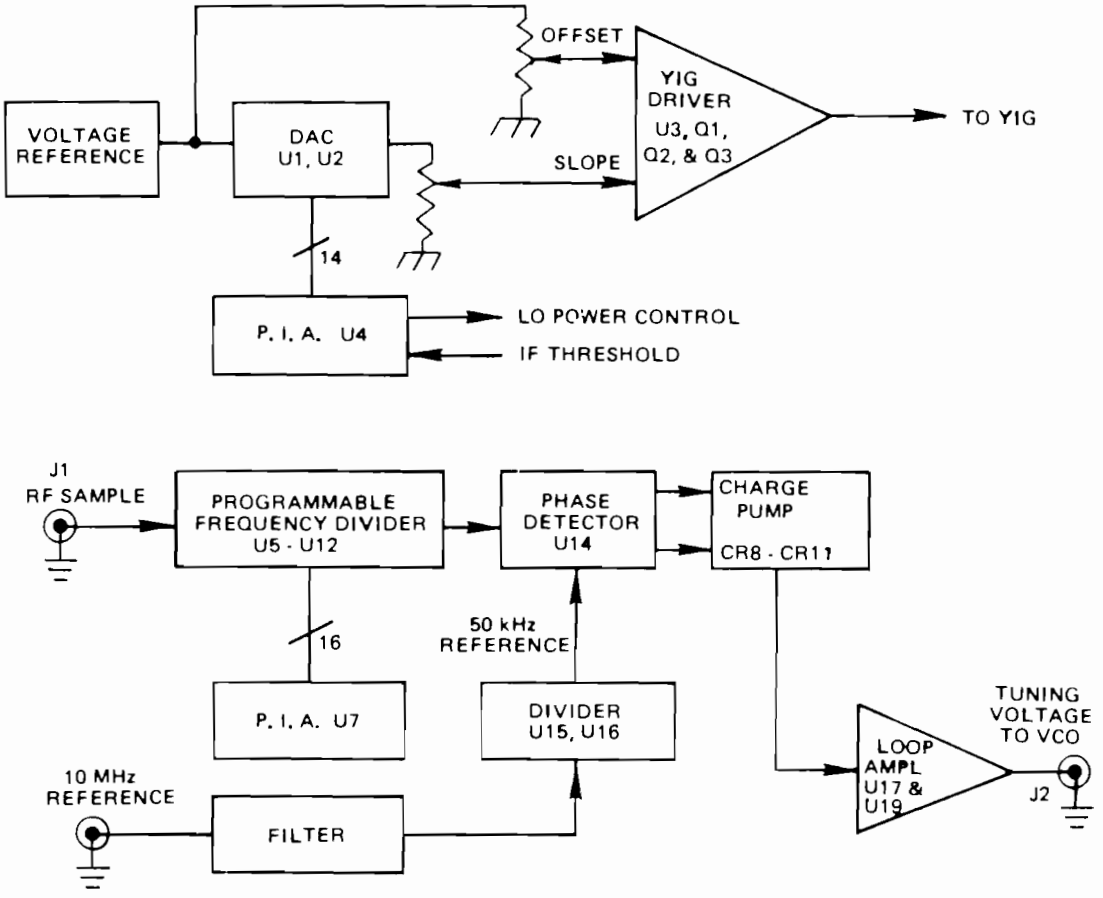


Figure 108-1. Converter Control Diagram

VCO CONTROL

The VCO control, together with the VCO, form a phase lock loop frequency synthesizer. The frequency range over which the synthesizer is used is from 370 MHz to 500 MHz.

An output of the VCO (via a buffer amplifier, U2, on the Band 2 converter board) is applied to the programmable frequency divider (U5-U13). The programmable frequency divider is programmed by the microprocessor via P.I.A. U7. The output of the programmable frequency divider is compared to the 50 kHz reference (derived from a 10 MHz clock from the gate generator board) in the phase detector U14. A phase difference between the divided down VCO and the 50 kHz reference will result in an output from the phase detector. The phase detector has two output ports, a pump-up port and a pump-down port. Pump-down is U14, pin 2. Pump-down is normally high and goes low to reduce the VCO frequency. Pump-up is U18, pin 3. Pump-up is normally low and goes high to increase the VCO frequency. The outputs of the phase detector go to the charge pump, which converts them to a single tri-state output. The charge pump output is open with no pump command, sources current with pump-up, and sinks current with pump-down. The output of the charge pump is connnected to the input of the loop amplifier U19 and U17. The loop amplifier provides the proper gain and filtering to achieve the desired loop response. The output of the loop amplifier is the VCO tuning voltage.

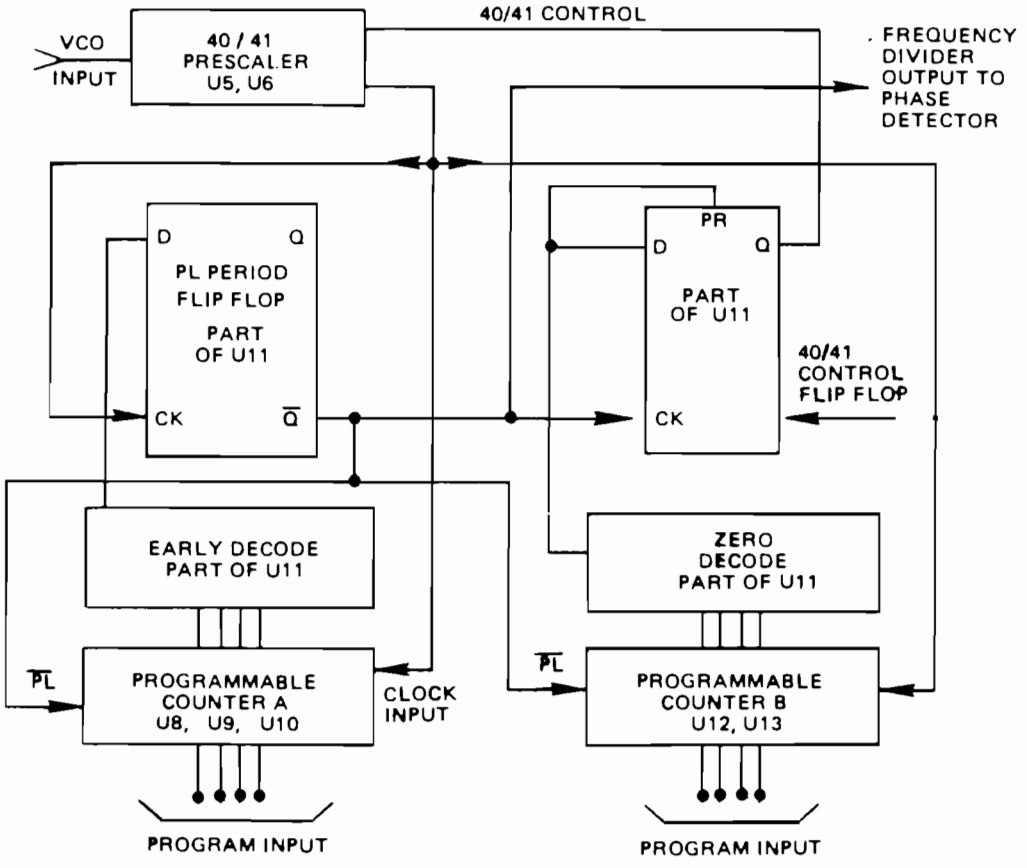


Figure 108-2. Programmable Frequency Divider Diagram

PROGRAMMABLE FREQUENCY DIVIDER

The programmable frequency divider uses a two modulus (divide number) prescaler (U5, U6) and two programmable counters (A & B). The prescaler is used to divide the VCO frequency down to a lower frequency which can be handled by low power Schottky TTL programmable counters. The two modulus prescaler permits prescaling without loss of resolution. At the start of the programmable frequency divider cycle, the prescaler is set to divide by the larger modulus (41), and both programmable counters have been loaded with their respective program numbers from the PIA. The programmable counters each decrement 1 count for each output pulse from the prescaler. When programmable counter B (U12, U13) reaches the count of zero the 40/41 control flip-flop (part of U11)changes state and causes the prescaler to divide by the lower modulus (40). When programmable counter A reaches the count of 2 the D input of the PL period flip-flop (part of U11) goes high, so that on the count of 1 the flip-flop changes state, which causes both programmable counters to be reloaded with their respective program numbers and the 40 41 control flip-flop to reset (prescaler in ÷ 41 state). The very next count causes the PL period flip flop to reset, starting the programmable frequency divider cycle over again. The equation for the divide ratio of the programmable frequency divider N_d is:

$$N_d = 40\ (N_{\text{counter A}}) + N_{\text{counter B}}$$

with the condition that:

$$N_{\text{counter B}} \text{ must not exceed } N_{\text{counter A}}$$

The weighting of the command bits is:

U9 P_1 – 400MHz	U10 P_1 – 4MHz
U9 P_0 – 200MHz	U10 P_0 – 2MHz
U8 P_3 – 160MHz	U13 P_3 – 1.6MHz
U8 P_2 – 80MHz	U13 P_2 – 0.8MHz
U8 P_1 – 40MHz	U13 P_1 – 0.4MHz
U8 P_0 – 20MHz	U13 P_0 – 0.2MHz
U10 P_3 – 16MHz	U13 P_1 – 100KHz
U10 P_2 – 8 MHz	U13 P_0 – 50KHz

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A108 CONVERTER CONTROL

2020200 04 B

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A108	CONVERTER CONTROL ASSY	2020200-02	1	EIP	34257
C1	Disc, .005μF, 20%, 100V	2150008	1	TG-D50	56289
C2	Disc, .01μF, 20%, 100V	2150003	14	TG-S10	56289
C3	Cer, X7R, .047μF, 10%, 50V	2150090	1	5020EM50RD473K	14158
C4	Tant, 1μF, 10%, 35V	2300008	3	TAPA 1 0M35	14433
C5	C4				
C6	C2				
C7	Disc, .001μF, 20%, 1KV	2150001	4	5GA-D10	56289
C8	C4				
C9	Tant, 33μF, 10%, 10V	2300015	2	TAPA 33M10	14433
C10 thru C12	C7				
C13 thru C17	C2				
C18	Tant, 10pF, 20%, 25V	2300029	4	DF106M25S	72136
C19	C18				
C20	C9				
C21	C18				
C22 thru C24	C2				
C25	Cer, Disc 560pF, 5%, 100V	2150029	2	SR211A561JAA	14158
C26	Tant, .47μF, 20%, 35V	2300005	1	TAPA-47M35	14433
C27	Cer, .022μF, 15%, 50V	2350027	1	2225L050X7R223K	26654
C28	C18				
C29	C2				
C30	Cer, Disc 330pF, 10%, 100V	2150030	1	SR211A331KAA	14158
C31	Tant, 2.2μF, 50%, 16V	2300012	1	TAPA 2-2M16	14433
C32	Mica, 82pF, 5%, 500V	2260032	2	CD10ED820J03	72136
C33	C2				
C34	Mica, SAT	2259999	1		
C35	Mica, 470 pF,5%, 500V	2250018	1	DM-15-471J	72136
C36	Mica, S.A.T.	2269999	1		
C37	Mono, .1μF, 10%, 50V	2150028	1	RC50104KB	51406
C38	C2				
C39	Mono, 2200pF, 5%, 100V	2150026	1	SR211A222JAA	14158
C40	C25				
C41	C2				
C42	C32				
CR1	Hot Carrier	2710004-00	1	5082-2835	28480
CR2	Zener, 56V	2704758-00	1	IN4758	07263
CR3	Fast Switch	2704148	14	IN4148	07263
CR4	Zener, 6.2V	2700827	1	IN827	07263
CR5	Power Rectifier	2704001	1	IN4001	07263
CR6 thru CR18	CR3				
L1	Inductor, 100μH	3520007	1	1537-76	99800
L2	Inductor, 1μH	3510018	1	1537-12	99800
L3	Inductor, 4700μH	3510017	2	1641-475	99800
L4	L3				
Q1	PNP, RF	4710009	1	MJE350	04713
Q2	PNP Amplifier	4710018	1	MPSL51	04713
Q3	NPN General Purpose	4704124	1	2N4124	04713

A108 CONVERTER CONTROL

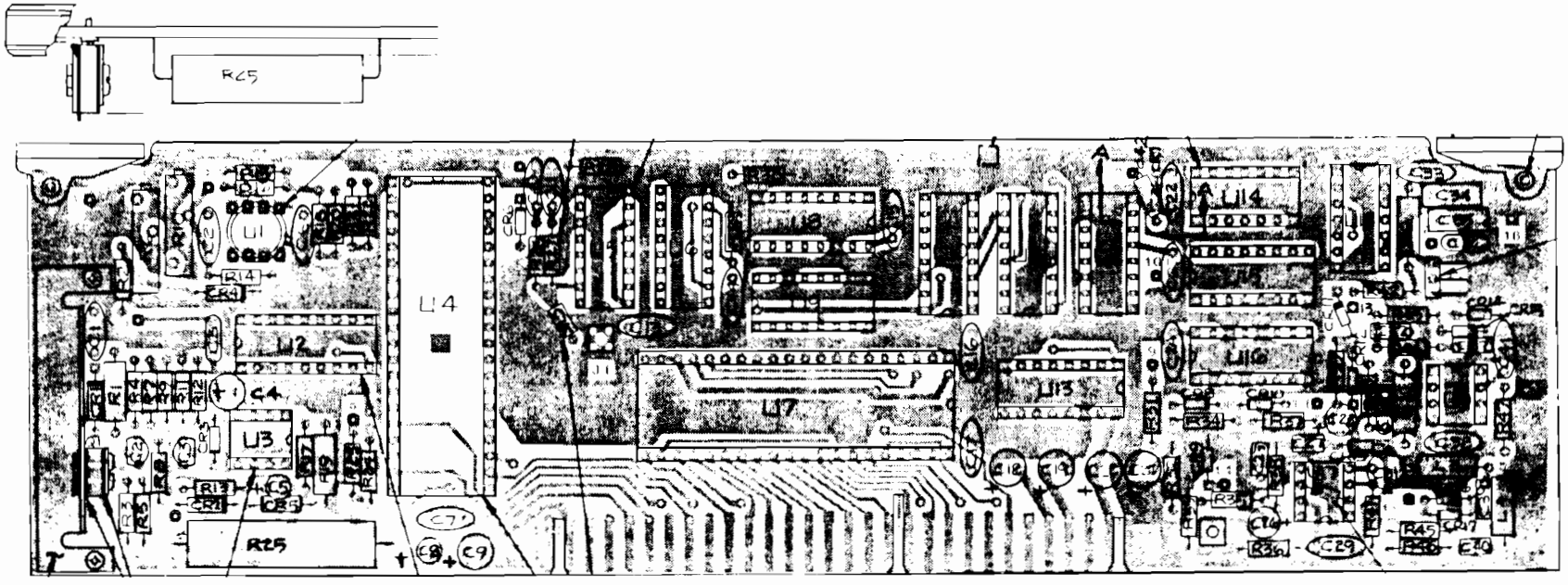
2020200-04 B

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R1	Res, PRCN 8.00K, 1/10W, 1%	4120022	1	0A-8.00K-10PPM-1%	02088
R2	Comp, 4.7K, 5%, 1/4W	4010472	1	RC07GF472J	81349
R3	Comp, 1K, 5%, 1/4W	4010102	6	RC07GF102J	81349
R4	Met Film, 49.9K, 1%, 1/10W	4054992	1	RN55C4992F	81349
R5	Met Ox, 390 ohm, 2%, 1/4W	4130391	2	C4/2%/390	24546
R6	Pot, WW	4280011	2	89PR-20K	73138
R7	Comp, 5.1M, 5%, 1/4W	4010515	1	RC07GF515J	81349
R8	R3				
R9	Met Ox, 10K, 2%, 1/4W	4130103	2	C4/2%/10K	24546
R10	R6				
R11	R9				
R12	Met Film, 1M, 1%, 1/10W	4051004	1	RN5SC1004F	81349
R13	R5				
R14	Comp, 750, 5% 1/4W	4010751	1	RC07GF751J	81349
R15	Comp, 820K, 5%, 1/4W	4010824	1	RC07GF824J	81349
R16	R3				
R17	Met Ox, 1.6K, 2%, 1/4W	4130162	1	C4/2%/1.6K	24546
R18	Comp, 1.60K, 5%, 1/4W	4010164	1	RC07GF164J	81349
R19	Prec, 3.01K, 1%, 1/10W	4120020	1	VAR-1/10C-6-1%	14298
R20	Comp, 10K, 5%, 1/4W	4010103	3	RC07GF103J	81349
R21	Comp, 82K, 5%, 1/4W	4010823	1	RC07GF823J	81349
R22	R20				
R23	R20				
R24	R3				
R25	Wire Wound 5, 1%, 7W	4110003	1	T7 (10 PPM)	12463
R26	Comp, 2.7K, 5%, 1/4W	4010272	1	RC07GF272J	81349
R27	Comp, 51, 5%, 1/4 W	4010510	2	RC07GF510J	81349
R28	Comp, 390, 5%, 1/4W	4010391	3	RC07GF391J	81349
R29	R28				
R30	R28				
R31	R3				
R32	Comp, 100, 5%, 1/4W	4010101	3	RC07GF101J	81349
R33	R3				
R34	Comp, 2.4K, 5%, 1/4W	4010242	1	RC07GF242J	81349
R35	R32				
R36	Comp, 220K, 5%, 1/4W	4010224	1	RC07GF224J	81349
R37	R32				
R38	Comp, 4.3K, 5%, 1/4W, NOM S.A.T.	4010999	1		
R39	Comp, 2K, 5%, 1/4W	4010202	1	RC07GF202J	81349
R40	R27				
R41	Comp, 1.5M, 5%, 1/4W	4010155	1	RC07GF155J	81349
R42	Comp, 300, 5%, 1/4W	4010301	1	RC07GF301J	81349
R43	Comp, 8.2K, 5%, 1/4W	4010822	1	RC07GF822J	81349
R44	Comp, 51K, 5%, 1/4W	4010513	2	RC07GF513J	81349
R45	Comp, 5.1K, 5%, 1/4W	4010512	1	RC07GF512J	81349
R46	R44				
R47	Comp, 3.3K, 5%, 1/4W	4010332	1	RC07GF332J	
U1	Prec, J-FET Op Amp	3041016	1	OP16FJ	06665
U2	12 Bit DAC	3050012	1	H57541-1	0000X
U3	Op Amp, Lin.	3040741	1	LM741CN	27014
U4	Peripheral Interface Adaptor	3086820	2	MC6820P	04713
U5	Two-Mod Prescaler	3112013-02	1	MC12013L	04713
U6	10K, M-S Flip-flop	3110131	1	MC10131L	04713
U7	U4				
U8 thru U10	UP/DOWN Counter	3084192	4	DM74LS192N	27014

A108 CONVERTER CONTROL

2020200-04 B

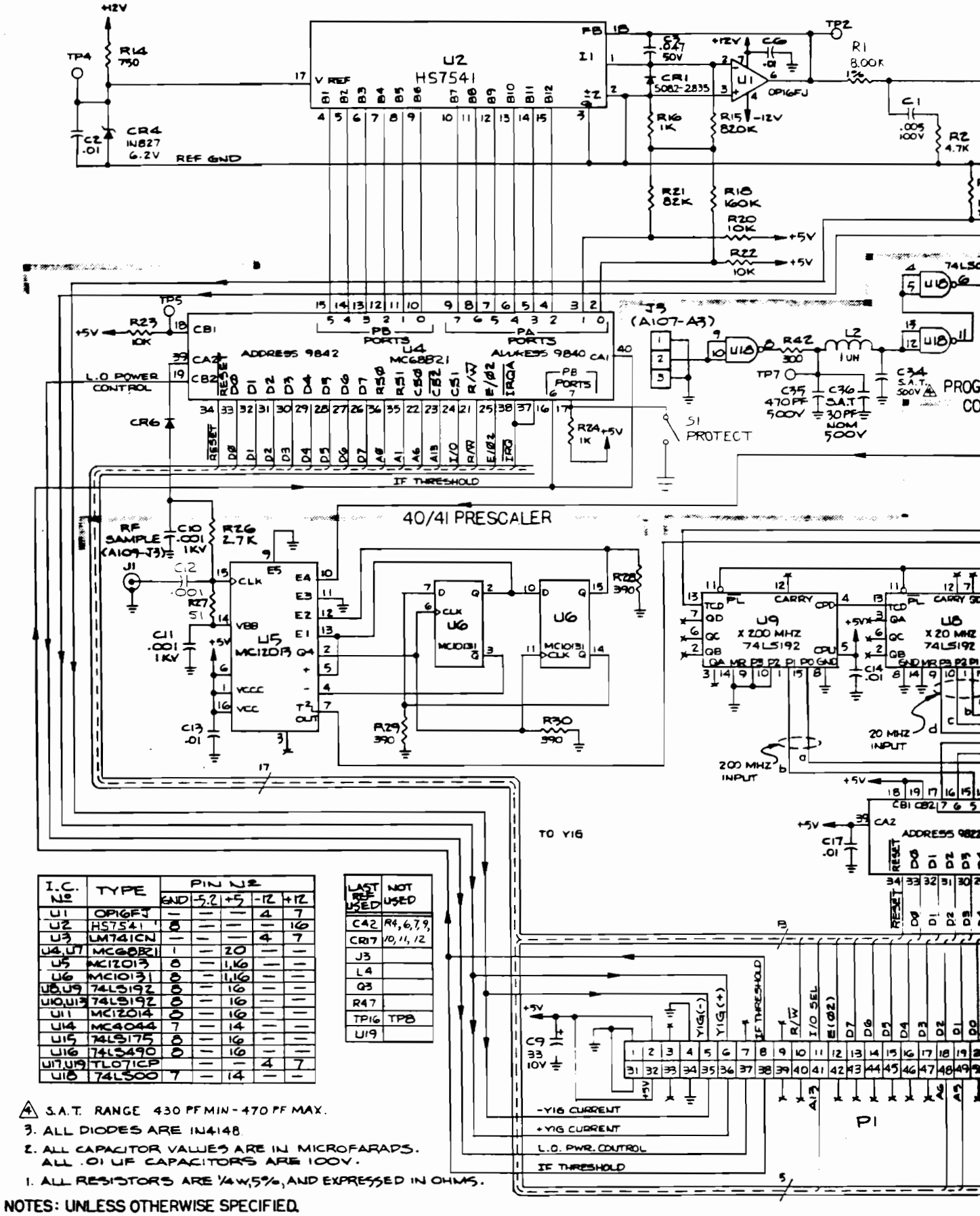
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
U11	Counter Control Logic	3112014	1	MC12014P	04713
U12	UP/DOWN Counter	3084193	1	DM74LS193N	27014
U13	U8				
U14	Phase Frequency Detector	3014044	1	MC4044P	04713
U15	Quad Dual Flip-flop	3084175	1	SN74LS175	01295
U16	Decade Counter	3084490	1	SN74LS490N	01295
U17	J-FET Op Amp	3040071	2	TL071CP	01295
U18	Quad 2 INP NAND	3087400	1	DM74LS00	27014
U19	U17				
J1	Mini P.C. Jack	2610038	2	51-451-0000	98291
J2	J1				
J3	RT. Angle, 3 Pin	2620132	1	22-05-2031	27264
S1	Switch, Dip, SPDT	4540007	1	435469-9	51216



2020200-04 B

Figure 108-3. Converter Control Component Locator

VOLTAGE REF

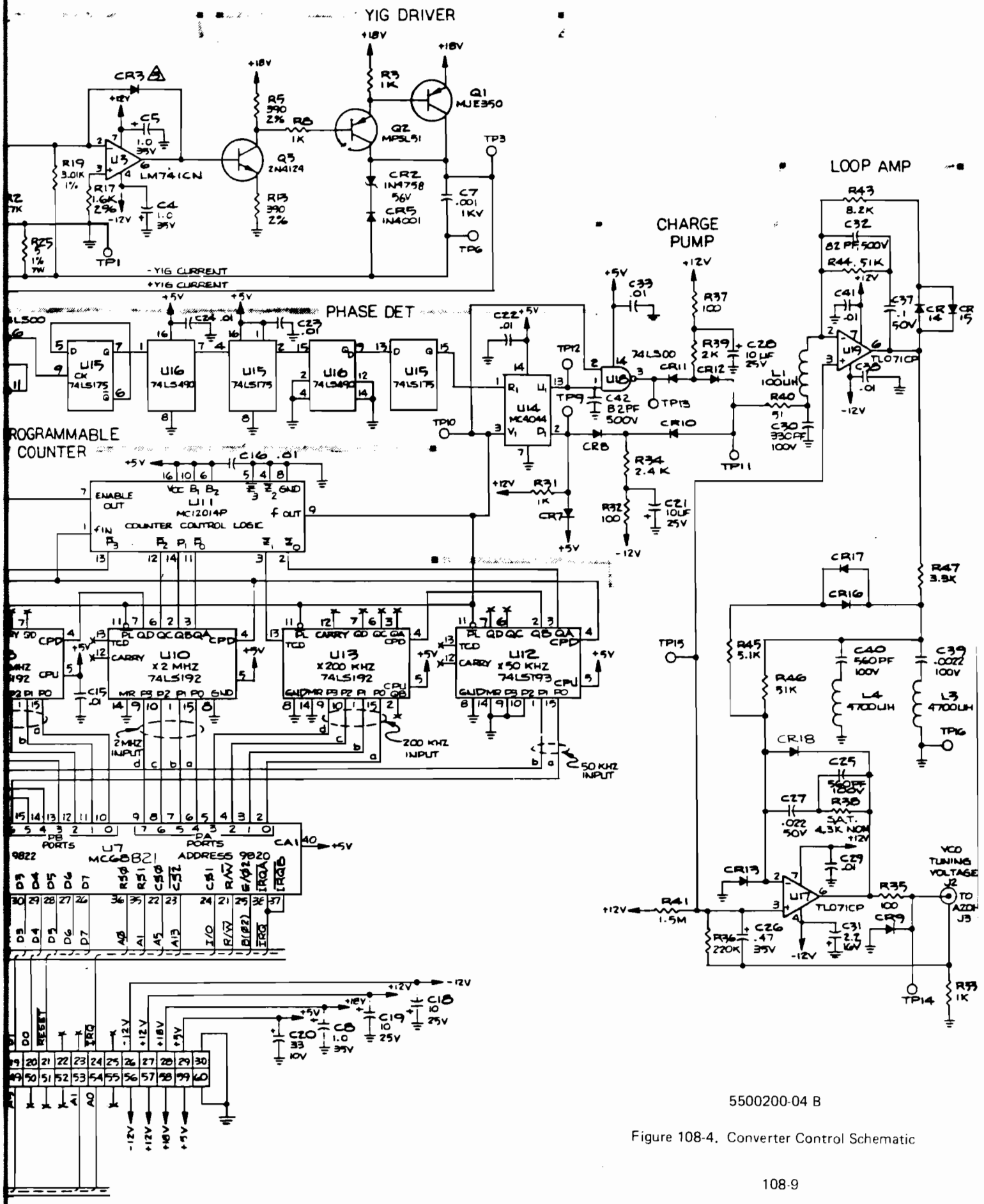


I.C. No	TYPE	PIN NO				
		GND	-5.2	+5	-12	+12
U1	OP16FJ	—	—	—	4	7
U2	HS7541	8	—	—	—	16
U3	LM741CN	—	—	—	4	7
U4,U7	MC6882I	1	—	20	—	—
U5	MC12013	8	—	1,16	—	—
U6	MC10131	8	—	1,16	—	—
U8,U9	74LS192	8	—	16	—	—
U10,U13	74LS192	8	—	16	—	—
U11	MC12014	8	—	16	—	—
U14	MC4044	7	—	14	—	—
U15	74LS175	8	—	16	—	—
U16	74LS490	8	—	16	—	—
U17,U19	TL071CP	—	—	—	4	7
U18	74LS00	7	—	14	—	—

LAST REF USED	NOT USED
C42	R4,6,7,9,
CR17	10, 11, 12
J3	
L4	
Q3	
R47	
TP16	TP8
U19	

4. S.A.T. RANGE 430 PF MIN - 470 PF MAX.
3. ALL DIODES ARE IN4148.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS. ALL .01 UF CAPACITORS ARE 100V.
1. ALL RESISTORS ARE 1/4 W, 5%, AND EXPRESSED IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED.



5500200-04 B

Figure 108-4. Converter Control Schematic

A109
BAND 2 CONVERTER
(2020139)

The Band 2 Converter accepts Band 1 and Band 2 RF signals from the front panel, and local oscillator (LO) signal from the Band 3 Converter (A203). The appropriate signal is selected and processed to produce an IF signal between 10 Hz and 200 MHz. The IF signal output is sent to the Count Chain board (A106), and lock information is routed through the PIA (peripheral interface adapter) U2 to the Microprocessor (A105).

IMPEDANCE CONVERTER

Band 1 input from the front panel enters the converter at J6 and is terminated by R75. The signal is coupled to the input of a field effect transistor (FET) amplifier (Q15) through an RC network (R73, C42). Two limiter diodes (CR4, CR5) protect the FET against large input signals. The FET is a source follower with slightly less than unity gain. The FET drives a buffer amplifier (Q14) which has enough gain to increase the impedance converter overall gain to near unity. A decoupling capacitor (C39) controls the amplifiers low frequency cutoff, and C41 provides high frequency peaking to keep the gain flat to frequencies above 100 MHz.

SIGNAL SELECT

The output of the impedance converter circuit drives one input of the signal select circuitry. Signal selection is made by enabling one of three differential amplifiers, U4A, U4B, or U5A. When Band 1 is selected, a logic high signal on the PIA (U2 pin 2) turns on Q16. Q16 biases on the current source in U4A. This current source generates an 11mA current which is split between the two differential amplifier transistors in U4A. The currents from pins 5 and 6 flow through matched collector loads (R94, L7/R95, L8). R94 and R95 are equal, and are selected for the proper low frequency gain during board alignment. Inductors L7 and L8 provide peaking to give an approximate flat gain through 200MHz. Diodes CR9 and CR10 provide limiting on very strong signals to prevent the next stage from being over driven.

The next stage is a differential amplifier similar to U4A, but it is driven differentially. To generate a single ended output signal, one output of U5B (pin 12) is passed through a current mirror (Q18). The output of the current mirror is then added to the second output of U5B (pin 11) at J5. The load for this stage is a 51 ohm resistor located on the A106 Count Chain board in order to terminate the coax for RF signals. In the quiescent state, the current from Q18 equals the collector current of the differential amplifier U5B, and the output current is zero. When a signal is applied, the current will be unbalanced to generate a signal at the load resistor. To provide frequency compensation of the current mirror, an RC network (R108, C34) is connected between the emitter of Q18 and ground.

BAND 1 LOCK DETECTOR

The output signal at J5 is coupled to detector CR12. Amplifier U6 is a threshold comparator that will produce a logic low signal when the IF output from J5 is more than −6dBm. The output of U6 goes through a resistor divider network to generate a 5V TTL logic signal for the PIA. R90 provides about 1 dB of positive feedback at threshold level to prevent erratic output from the comparator.

ISOLATION AMPLIFIER

The Band 2 input signal enters on J4. This RF signal is terminated in 50 ohms by the combination of R1 and the input impedance of the amplifier. The input signal level is detected by CR1, filtered by C3, and applied to one input of the Band 2 lock detector (U1).

The isolation amplifier is a common base amplifier with a gain of −10 dB. An input signal range of +10 to −20dBm is translated to a 0 to −30dBm range into the mixer so the mixer will be in its linear range for all signal input levels. The amplifier peaks slightly near 1 GHz to overcome an increase in mixer conversion loss at these frequencies.

MIXER OPERATION

The local oscillator (LO) is applied to the IF terminal and the IF is removed from the LO terminal. This swap allows the mixer (MX1) to be unbalanced and act as a low loss attenuator for signals between 10MHz and 200MHz where no mixing is necessary. The mixer has a nominal 400MHz LO for signals between 200MHz and 600MHz; and has a nominal 800MHz LO for signals between 600MHz and 1GHz. A 980MHz LO allows operation with input signals to 1160MHz.

IF AMPLIFIER

The output of the mixer drives an IF amplifier through a 7 section, 200MHz low-pass filter. The IF amplifier is a "feedback pair" amplifier whose gain is stabilized by feedback, to be equal to 24dB. Inductor L6 is used to extend the high frequency response to 200MHz. The 1 pF capacitor (C26) between R34 and R35 is a low pass filter to reduce the 1200 to 1500 MHz LO harmonics that reach the IF amplifier.

BAND 2 LOCK DETECTOR

The IF amplifier output goes to the signal select circuit and to the Band 2 Lock Detector. The Band 2 Lock Detector has a voltage proportional to the IF level on the positive input, and a voltage proportional to the RF signal on the Negative input. The conversion gain from RF input to IF amplifier output is a +6dB for all valid signals, and less than −6dB for all spurious signals. The output of U1 is positive only when a valid IF signal is present. A small offset is added by R12 and R13 to guarantee a non lock condition when no signal is present. Resistor R90 provides about 1dB of positive feedback to prevent erratic output from noise at the point of threshold.

LO BUFFER

The VCO signal from the Band 3 Converter (A201A, J2) enters on J1. The signal goes through a 6 dB attenuator (R111, R112, R114), and a low pass filter (L1, C63, C64 to attenuate high order harmonics), and is terminated by a 51 ohm resistor (R16). Two high input impedance signal splitters (Q2, Q3) get their input signals from R16. Q2 and Q3 operate on the same basic principal. One output is taken from the emitter (acting as an emitter follower) which provides unity gain for the input signal. The AC terminating impedance on the emitter is adjusted to be 50 ohms so the amplifier will act as a unity gain amplifier for the 50 ohm load which terminates the collector when a coax cable is connected. U2 has an additional transformer (T1) in its collector lead to increase the signal output to J3 by about 4 dB.

DIVIDE-BY-TWO

The emitter output of Q3 drives the input of a divide-by-two IC (U3). The impedance is held at 50 ohms by two terminating/biasing resistors (R61, R62). The resistors keep the input bias to U3 below the emitter-coupled logic (ECL) low level (approx. −2.0V). The microprocessor enables self-test by putting a low level signal on pin 5 of the PIA (U2). This turns on Q13, and raises the voltage at U3 pin 7 to the center of an ECL signal (approx. −1.2V). This allows U3 to divide the input signal by two. The output of U3 goes to the signal select circuits.

LO SELECT

The signal from the emitter of Q2 drives the LO select circuitry. The LO provides one (of three) signals to the mixer (MX1). In Band 2A a bias current is generated to unbalance the mixer and allow signals below 190MHz to pass. In Band 2B a 370MHz or 425MHz LO signal is generated that will mix with signals of 200 to 600MHz, and provide the 10 to 200MHz IF signal desired. In Band 2C a 750MHz, 850MHz or 980MHz LO signal is generated to mix with input signals between 600MHz and 1160MHz to provide the desired IF signal.

In Band 2A, the 3mA current to bias mixer MX1 is generated when Q12 is turned on by the PIA, to apply +12V to MX1 through R57. This will allow signals to pass that are less than the cutoff frequency of the low pass filter (200MHz). The LO signal to mixer MX2 from Q2 is not allowed to pass MX2 because of the inherent balance of the mixer. No signal can enter pin 2 of MX2 because Q7 has been saturated, removing bias from buffer Q5, and shunting any RF signals to ground.

When Band 2B is selected, Q12 is turned off thus balancing mixer MX1; Q6 is turned on to unbalance mixer MX2. With MX2 unbalanced, the LO signal from Q2 can pass through MX2 and be amplified by Q10 and Q11, and be applied to mixer MX1.

When Band 2C is selected both Q6 and Q12 are off, and both mixers are balanced. In this mode Q7 is shut off and an LO signal is applied to pin 1 and 2 of MX2. The sum output of MX2 is selected by a DC blocking capacitor (C31). This sum (that is two times the incoming LO frequency) is amplified by Q10 and Q11 and applied to MX1.

The Q10 and Q11 amplifier is a series shunt pair. Q10 applies most of the RF input signal across the emitter resistor R47. This determines the transistor emitter current, which will be the collector current if the output is terminated in a low impedance. Q11 is used as a current-to-voltage converter. The output voltage of this converter is the product of the input current times the feedback resistor (R51). Since the input of this stage is a summing junction, it appears very close to zero ohms to the previous stage, Q10. The voltage gain of the two transistors can be approximated by R51/R47, which is about 3 or 10dB. Since the gain required at 800MHz is slightly greater than required at 400MHz, a low pass matching network (consisting of L2 and C20) peaks the output signal current to MX1 at 800 MHz. The remaining components around Q10 and Q11 are used to bias the transistors. Shunt biasing is used to provide collector bias voltages of 3.4V for Q10, and 4.7V for Q11.

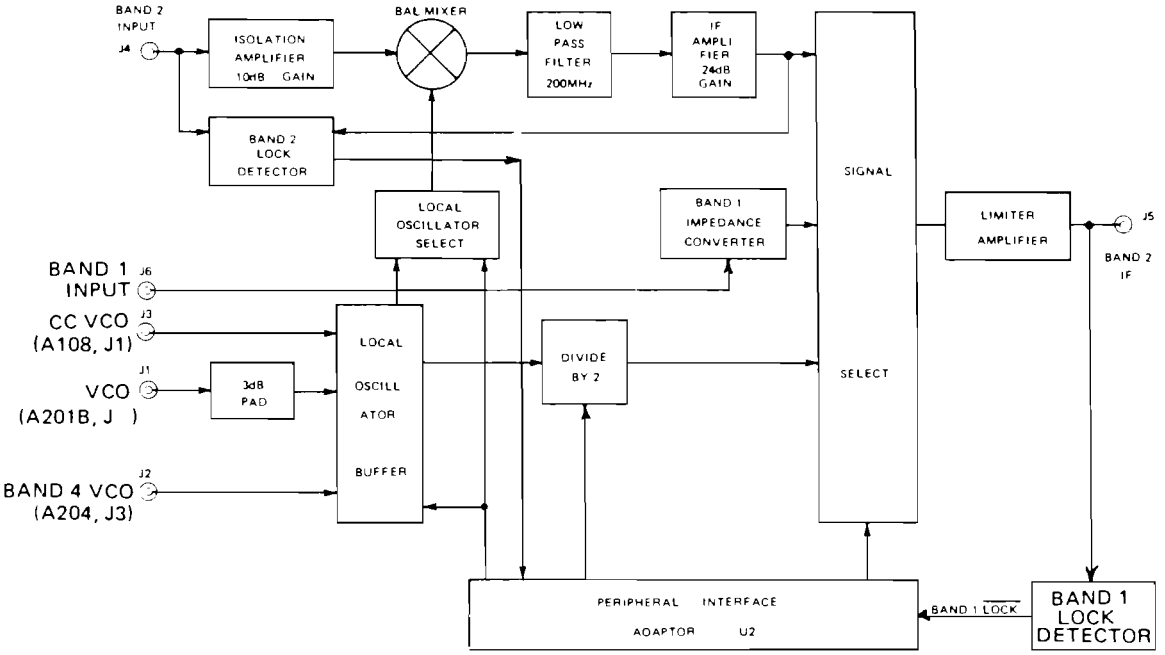


Figure 109-1. Band 2 Converter Block Diagram

A109 BAND 2 CONVERTER

2020139-05,06 A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A109	Band 2 Converter Assy	2020139-03	1	EIP	34257
C1	Cer, .01μF, 10%, 100V	2150014-00	9	6123X7R103KA100	26654
C2	C1				
C3	Cer, .001μF 10%, 100V	2150015	11	6183X7R102KA100	26654
C4 thru C6	C1				
C7	Mica, 100pF, 5%, 500V	2260034	3	FD101J03	72136
C8	Disc, .001μF, 20%, 1KV	2150001	8	SGA - D10	56289
C9	Disc, .01μF, 20%, 100V	2150003	11	TG - S10	56289
C10	C8				
C11	C8				
C12	C7				
C13	C8				
C14	C7				
C15 thru C18	C3				
C19	C8				
C20	Mica, 1pF, 5%, 500V	2260005	2	CD010C03	56289
C21	Mica, 18pF, 5%, 500V, NOM - S.A.T	2260999	3	CD180J03	56289
C22	Mica, 33pF, 5%, 500V, NOM - S.A.T.	2260999	2	ED330J03 (2260021)	56289
C23	C22				
C24	Mica, 27pF, 5%, 500V NOM S.A.T.	2260999	1	CD180J03	56289
C25	C1				
C26	C20				
C27	Not Used				
C28	C1				
C29	C9				
C30	C1				
C31	C3				
C32	C3				
C33	C1				
C34 thru C36	C3				
C37	C9				
C38	C3				
C39	Tant, 100μF, 20%, 6.3V	2300024	1	TAG20 - 47/6.3 - 50	14433
C40	C9				
C41	Mica, 22pF, 5%, 500V	2660017	1	ED220J03	72136
C42	Mica, 47pF, 5%, 500V	2260004	1	DM10 - 470J	72136
C43	Tant, 33μF,10%, 10V	2300015	6	TAG20 - 33/10 - 50	14433
C44	C9				
C45	C43				
C46	C8				
C47 thru C49	C9				
C50	Tant, 10μF, 20%, 25V	2300029	3	TAG20 - 10/25	14433
C51	C43				
C52	C9				
C53	C9				
C54	Mica, 18pF, 5%, 500V	2260015	1	CD180J03	56289
C55	C8				
C56	C8				
C57	C50				

A109 BAND 2 CONVERTER, continued

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REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
C58	C43				
C59	C9				
C60	C43				
C61	C50				
C62	C43				
C63	Mica, 8pF, 13%, 500V	2660011	2	CD080J03	56289
C64	C63				
CR1	Mix UHF	2710038	3	ND4991	00005
CR2	Not Used				
CR3	CR1				
CR4	Fast Switch, General Purpose	2704148	3	1N4148	07263
CR5	CR4				
CR6 thru CR10	Not Used				
CR11	CR4				
CR12	CR1				
L1 thru L5	Part of Board				
L6	Inductor, 0.47 =H	3510006	1	DD - 0.47	99800
L7	L1				
L8	L1				
MX1	Balanced Mixer	2030016	2	TFM- 2	
MX2	MX1				
Q1	NPN, RF	4710030	8	BFR-90	04713
Q2	Q1				
Q3	Q1				
Q4	PNP, General Purpose	4704124	1	2N4124	04713
Q5	Q1				
Q6	PPNP, General Purpose	4704126	7	2N4126	04713
Q7	Q1				
Q8	Q1				
Q9	Q1				
Q10	NPN,RF, graded	4710030-02	1	BFR-90	
Q11	Q1				
Q12	Q6				
Q13	Q6				
Q14	PNP, RF (mod)	5280047	2	2N4261 T072	04713
Q15	NN-Channel, JFET	4704416	1	2N4416	04713
Q16	Q6				
Q17	Q6				
Q18	Q14				
Q19	Q6				
Q20	Q6				
R1	Comp, 150, 5%, 1/8 W	4000151	1	RC05GF151J	81349
R2	Res, MF, 75.0, 1%, 1/8W	4067509	1	RN55D7509F	91637
R3	Res, 1.1K, 5%, 1/4 W	4130112	1	C4/2%/10	24546
R4	Res, 820, 2%, 1/4 W	4130820	4	C4/2%/820	24540
R5	Comp, 33, 5%, 1/8 W	4000330	1	RC05GF330J	81349
R6	Comp, 51, 5%, 1/8 W	4000510	1	RC05GF510J	81349
R7	Comp, 10K, 5%, 1/4 W	4010103	3	RC07GF103J	81349
R8	Met Ox, 8.2K, 2%, 1/4 W	4130822	2	C4/2%/8.2K	81349
R9	Met Ox, 30K, 2%, 1/4 W	4130303	1	C4/2%/30K	24546
R10	Met Ox, 43K, 2%, 1/4 W	4130433	2	C4/2%/43K	24546
R11	Comp, 43K, 5%, 1/4 W	4010433	1	RC07GF433J	81349
R12	Met Ox, S.A.T., Nom, 15K	4130999	4	C4/2%/15K	24546
R13	Met Ox, 12.1, 1%, 1/8W	4061219	1	RN55D1219F	91637

A109 BAND 2 CONVERTER, continued

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R14	Comp, 36, 5%, 1/4 W	4010360	1	RC07GF36J	81349
R15	Comp, 11, 5%, 1/4 W	4010110	2	RC07GF110J	81349
R16	Met Ox, 51.1, 1%, 1/8W	4065119	2	RN55D51R1F	91637
R17	Comp, 1K, 5%, 1/4 W	4010102	4	RC07GF102J	81349
R18	R4				
R19	R15				
R20	Res, CC,1/4W, 5%, SAT	4010999	1		
R21	Comp, 220, 5%, 1/4 W	4010221	2	RC07GF221J	81349
R22	Comp, 20K, 5%, 1/4 W	4010203	1	RC07GF203J	81349
R23	Res, CC, 820, 1/4W, 5%	4010821	2	RC07GF821J	19020
R24	Comp, 10, 5%, 1/8 W	4010100	11	RC07GF100J	81349
R25	Met Ox, 750, 2%, 1/4 W	4130751	2	C4/2%/750	24546
R26	Comp, 11k, 5%, 1/4 W	4010113	3	RC07GF113J	81349
R27	Met Ox, 4.7K, 2%, 1/4 W	4130472	1	C4/2%/4.7K	24546
R28	Met Film33.2, 1%, 1/8W	4063329	2	RN55D3329F	91637
R29	Comp, 4.7K, 5%, 1/4 W	4010472	2	RC07GF472J	81349
R30	R26				
R31	Comp, 8.2K, 5%, 1/4 W	4010822	2	RC07GF822J	81349
R32	R7				
R33	R7				
R34	Met Film 27.4, 1%, 1/8W	4062749	1	RN55D2749F	91631
R35	Met Film 24.3, 1%, 1/8W	4062439	1	RN55D24R3F	91631
R36	R24				
R37	Comp, 10, 5%, 1/8 W	4000100	1	RC05GF100J	81349
R38	R17				
R39	R4				
R40	R4				
R41	R24				
R42	R16				
R43	R24				
R44	Comp, 910, 5%, 1/4 W	4010911	1	RC07GF911J	81349
R45	Comp, 3.9K, 5%, 1/4 W	4010392	3	RC07GF392J	81349
R46	Comp, 27K, 5%, 1/4 W	4010273	1	RC07GF273J	81349
R47	R28				
R48	Comp, 3.3K, 5%, 1/4 W	4010332	1	RC07GF332J	81349
R49	Comp, 390, 5%, 1/4 W	4010391	1	RC07GF391J	81349
R50	Comp, 13K, 5%, 1/4 W	4010133	1	RC07GF133J	81349
R51	Met Film121, 1%, 1/8W	4061210	1	RN55D1210F	24546
R52	R24				
R53	R31				
R54	R26				
R55	R25				
R56	R24				
R57	R12 (4.3K Nom)	4130999	1	C4/2%/4.3K	
R58	R17				
R59	R45				
R60	R12 (300 or 560 NOM)	4130999	1	C4/2%/560	
R61	Met Film 82.5, 1%, 1/8W	4068259	1	RN55D82R5F	24546
R62	Met Film130.0, 1%, 1/8W	4061300	2	RN55D1300F	24546
R63	Comp, 510, 5%, 1/4 W	4010511	1	RC07GF511J	81349
R64	Comp, 51, 5%, 1/4 W	4010510	2	RC07GF510J	81349
R65	Comp, 200, 5%, 1/4 W	4010201	1	RC07GF201J	81349
R66	Comp, 160K, 5%, 1/4 W	4010164	1	RC07GF160K	81349
R67	Met Ox, 1.8K, 2%, 1/4 W	4130182	1	C4/2%/1.8K	24546
R68	R24				
R69	Met Ox, 510, 2%, 1/4 W	4130511	2	C4/2%/510	24546
R70	R12 (Nom 1.2K)	4130999	1	C4/2%/1.2K	24546
R71	R29				
R72	R24				

A109 BAND 2 CONVERTER, continued

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REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R73	Comp, 1M, 5%, 1/4 W	4010105	2	RC07GF105J	81349
R74	R64				
R75	R73				
R76	Met Ox, 2.2K, 2%, 1/4 W	4130222	3	C4/2%/2.2K	24546
R77	Met Ox, 3.9K, 2%, 1/4W	4130392	3	C4/2%/3.9K	24546
R78	Comp, 5.6K, 5%, 1/4 W	4010562	1	RC07GF562J	81349
R79	Comp, 3.6K, 5%, 1/4 W	4010362	3	RC07GF362J	81349
R80	Met Ox, 7.5K, 2%, 1/4 W	4130752	3	C4/2%/7.5K	24546
R81	R76				
R82	R24				
R83	Met Ox, 200, 2%, 1/4 W	4130201	3	C4/2%/200	24546
R84	R77				
R85	Met Ox, 330, 2%, 1/4 W	4130331	1	C4/2%/330	24546
R86	Comp, 6.8K, 5%, 1/4 W	4010682	2	RC07GF682J	81349
R87	R79				
R88	R80				
R89	R8				
R90	Comp, 75K, 5%, 1/4 W	4010753	1	RC07GF753J	81349
R91	Met Ox, 33K, 2%, 1/4 W	4130333	1	C4/2%/33K	24546
R92	Met Ox, 160, 2%, 1/4 W	4130161	1	C4/2%/161	24546
R93	R21				
R94	Met Film S.A.T.(1.2 NOM)	4069999	2	C4/2%/1.2	
R95	R94 (12.1 NOM)				
R96	R83				
R97	R83				
R98	R77				
R99	R86				
R100	R79				
R101	R80				
R102	R10				
R103	R76				
R104	Comp, 180, 5%, 1/4 W	4010181	1	RC07GF181J	81349
R105	R24				
R106	Met Film 90.9, 1%, 1/8W	4069099	1	RN55D9099F	91637
R107	R62				
R108	R24				
R109	R69				
R110	R17				
R111	Comp, 160, 5%, 1/4 W	4010161	2	RC07GF161J	81349
R112	R111				
R113	Met Film 20.0, 1%, 1/8W	4062009	1	RN55D2009F	91637
R114	Met Ox, 2K, 2%, 1/4 W	4130202	2	C4/2/2K	24546
R115	R114				
R116	Met Ox, 9.1K, 2%, 1/4 W	4130912	2	C4/2%/9.1K	24546
R1117	R116				
R118	Comp, 300K 5%, 1/4 W	4010301	1	RC07GF301J	81349
R119	R45				
R120	R23				
R121	Comp, 68, 5%, 1/4 W	4010680	1	RC07GF680J	23044
R122	Comp, 100K, 5%, 1/4 W	4010101	1	RC07GF100J	81349

A109 BAND 2 CONVERTER, continued

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REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
TP1 thru TP16	Conn, Pin, .04D	2620032	16	460 - 2970 - 02 - 03	71279
U1	Prec, JFET Op Amplifier	3041016	1	OP16FJ	06665
U2	Periph. Interface Adaptor	3086821	1	MC68B21P	04713
U3	750 MHz, D-Type Flip Flop	3001106	1	11C06	07263
U4	Dual/Diff. Amplifier	3043049	2	CA3049	27014
U5	U4				
U6	Op Amplifier	3040741	1	TIUA741CP	27014

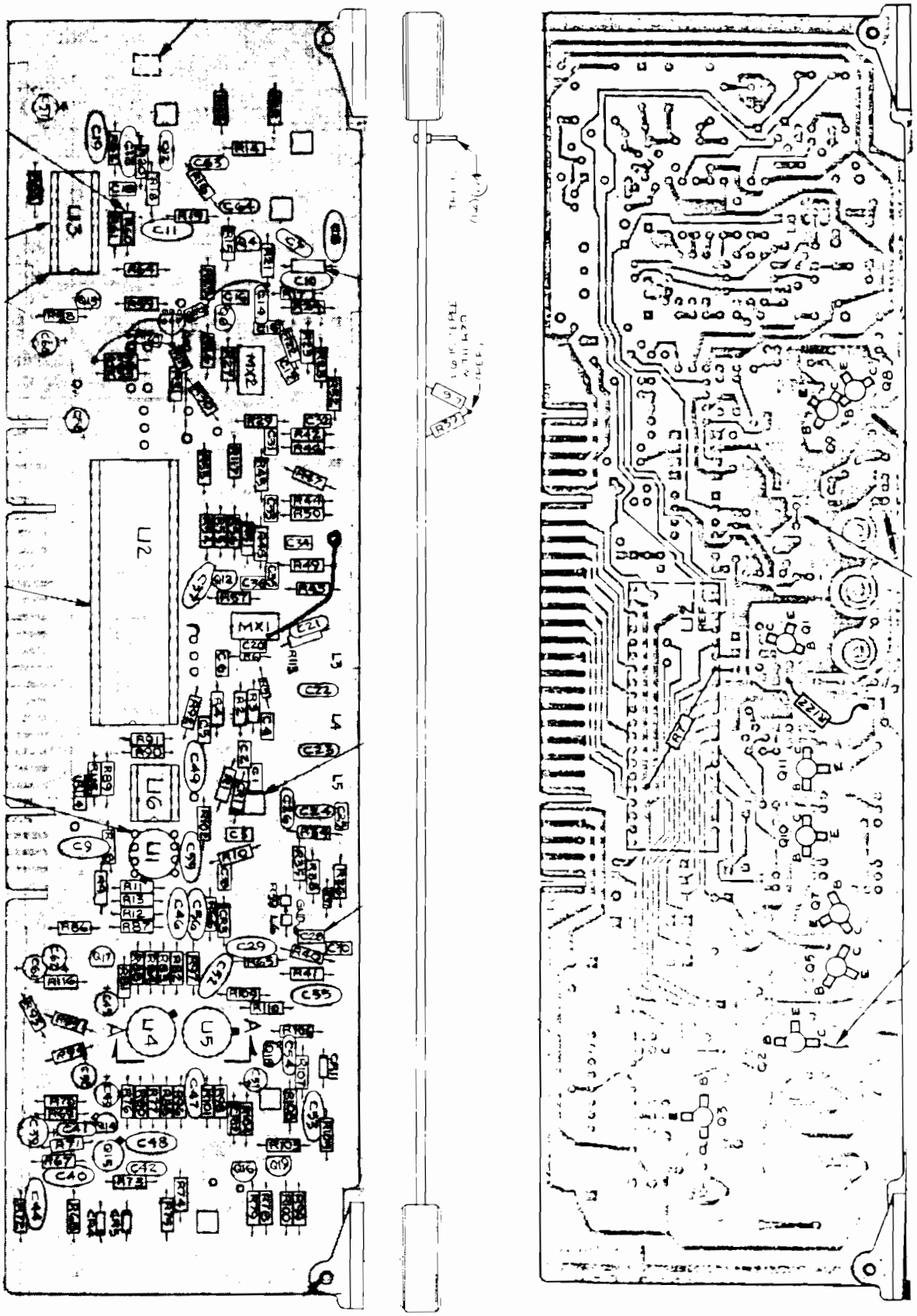

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Figure 109-2. Band 2 Converter Component Locator

A111
FRONT PANEL LOGIC
(2020191)

The Front Panel Logic assembly (A111) contains logic circuitry for control of two functions.

- DISPLAY CONTROL
- KEYBOARD CONTROL

The +5 V power supply to the front panel assemblies (A110 and A111) is regulated by a voltage regulator that is located behind the A111 board. For heatsinking purposes, this voltage regulator is mounted on the chassis. Please refer to Figure 111-2, Front Panel Logic block diagram, on page 111-3.

DISPLAY CONTROL

The twelve 7-segment LEDs and the three groups of annunciator lights on A110 are multiplexed. To turn on a particular segment in a digit, both the digit driver for that digit and the segment driver for that segment must be on.

The display logic is in constant operation in either the self-scan mode or the memory update mode.

SELF-SCAN MODE

This is the normal operating mode. In this mode the display scan clock is clocking the display counter (U6). The state of the display counter determines which digit will be turned on.

The state of the display counter is decoded by 4 to 16 line multiplexer (U2), and the appropriate digit driver is turned on. At this time the display memory (U7 and U8) is read, and the on/off information (stored in the display memory for that specific digit), turns the segment drivers (A110) on or off.

The display intensity is controlled by varying the duty cycle of the multiplexing. This is done by varying the resistance of the potentiometer (R4) which, in turn, varies the length of time the decoder (U2) and the display memories (U7, U8) are disabled between each scan clock cycle.

At the start of each gate operation, the GATE light control is triggered, and the GATE LED lights for the length of the gate.

MEMORY UPDATE MODE

In this mode the multiplexer logic is disabled by setting the display scan/$\overline{\text{update}}$ control line (PA4) to logic 0. The microprocessor controlled clock ($\overline{\text{clock}}$, PA1) is used to clock the display counter(U6).

Before updating the display memory (U7 and U8), the display counter is cleared by setting the clear/load control line (PA5) to logic 1, and clocking the clock input of U6. Update mode timing is illustrated in figure 111-1.

KEYBOARD CONTROL

When the keyboard is not being read by the microprocessor, the Keyboard READ/$\overline{\text{SCAN}}$ control line (PA0) is at logic 0. All the outputs of the shift register are at logic 0. If no key on the keyboard is pushed, all the inputs to the 8-input NAND gate (U13) are at logic 1 level. When a key is pushed, the column containing that key will be grounded. The output of U13 goes to logic 1 and C7 (in the debounce circuit) starts to discharge. When the voltage across C7 reaches approximately +0.7 V above ground, the debounce circuit will trigger the interrupt input on the PIA (U11, pin 18) indicating that a key is being pushed.

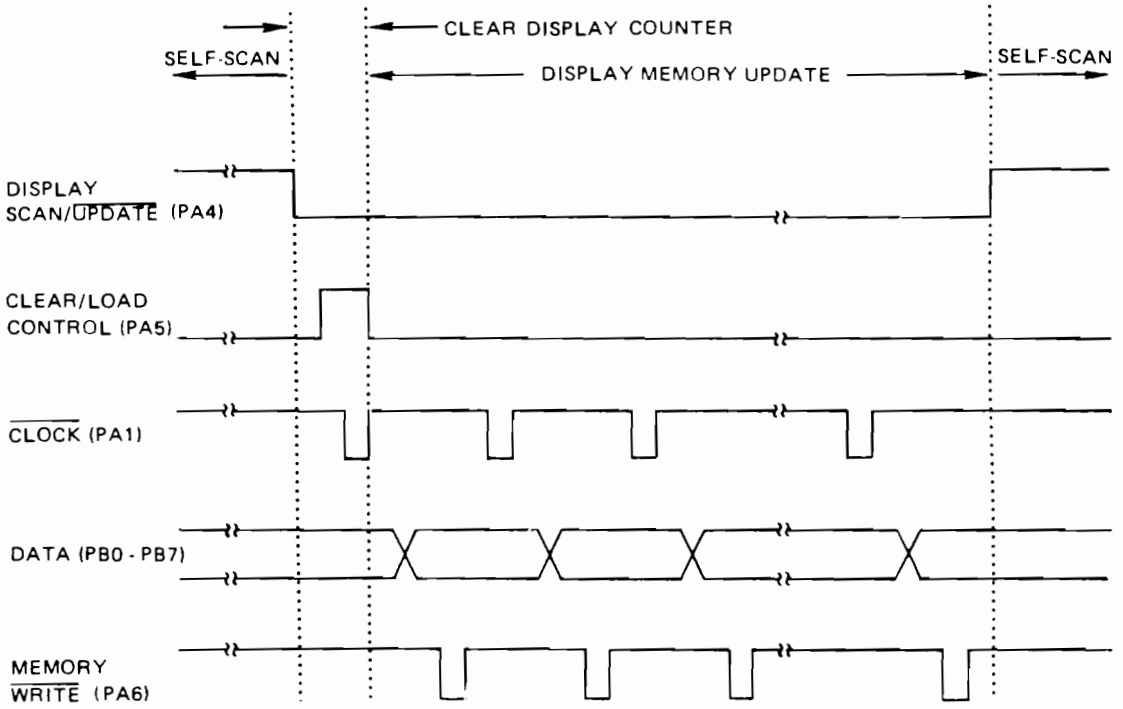

Figure 111-1. Memory Update Mode Sequence

READ KEYBOARD

When the microprocessor needs to read the keyboard, a logic 1 is put on the keyboard READ/$\overline{\text{SCAN}}$ control line (PA0). This enables the data buffer (U9). A 0111 is then loaded into the shift register (U3) by putting a logic 1 on the CLEAR/LOAD control line (PA5) and clocking the clock input of U3. The logic 0 at the output of the shift register (U3) is shifted through the shift register once. The microprocessor reads the keyboard row and column information with the logic 0 at each of the 4 outputs of U3 to determine the coordinate of the key pushed. After the keyboard is read, the keyboard READ/$\overline{\text{SCAN}}$ line is returned to logic 0.

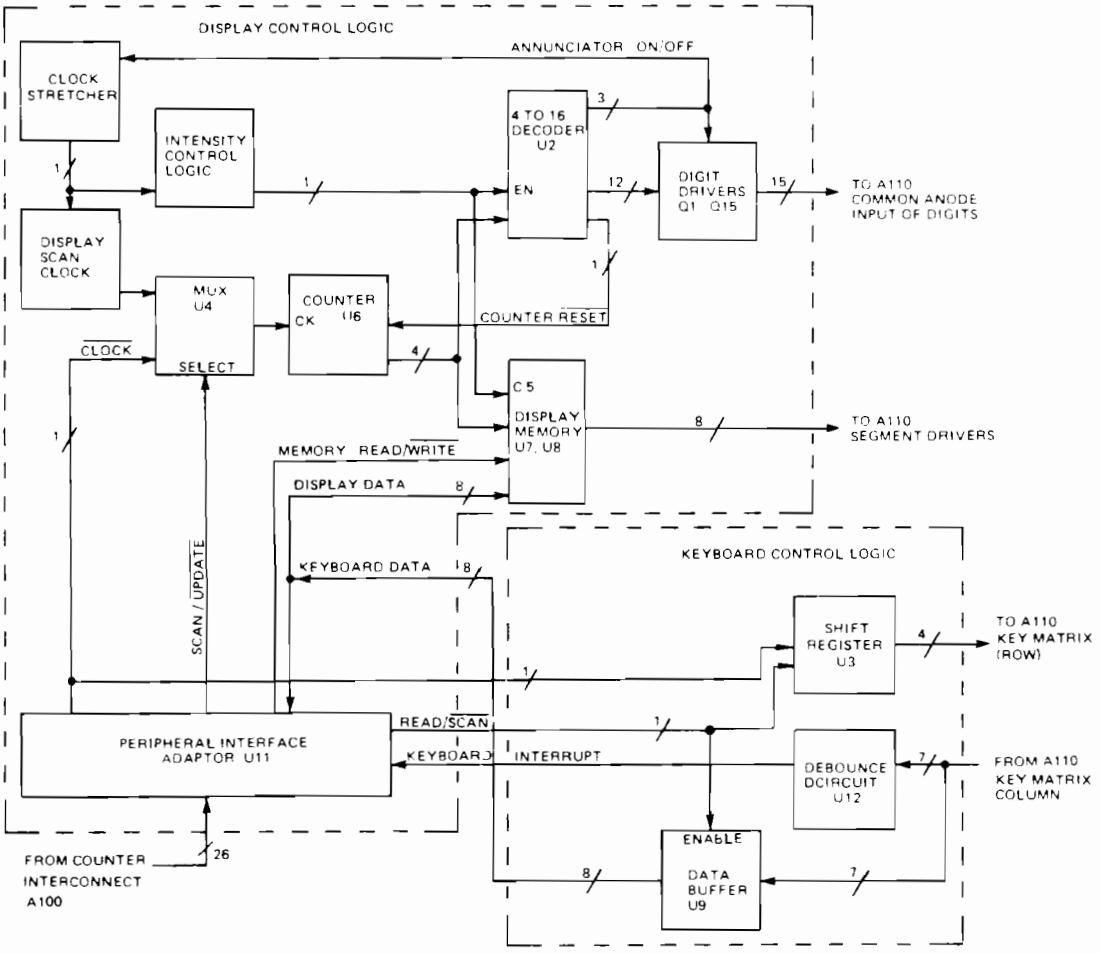

Figure 111-2. Front Panel Logic Block Diagram

A111 FRONT PANEL DRIVER

2020191-02 A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A111	Front Panel Driver Assy	2020191	1	EIP	34257
C1	Tant, 0.1μF, 10%, 35V	2300020	1	TAPA .10M35	14433
C2	Cer., .002μF, 20%, 1KV	2150005	2	TG - S20	56289
C3	C2				
C4	Not Used				
C5	Tant, 47μF, 20%, 16V	2300025	1	TAPA 47M16	14433
C6	Tant, 2.2μF, 20%, 16V	2300012	1	TAPA 2.2M16	14433
C7	Tant, 22μF, 20%, 16V	2300030	1	TAPA 22M16	14433
C8	Tant, .33μF, 20%, 35V	2300031	1	TAPA .33M16	14433
C9	Tant, 33μF, 20%, 10V	2300015	1	TAPA 33M16	14433
C10 thru C15	Cer., .01μF, 20%, 100V	2150003	6	TG - S10	56289
CR1	Fast Switch	2704148	1	IN4148	07263
J1	9 Pin Male	2620062	1	22 - 03 - 2091	0000B
J2	17 Pin Male	2620064	1	22 - 03 - 2171	0000B
J3	13 Pin Male	2620063	1	22 - 03 - 2131	0000B
J4	4 Pin, FR. LOCK	2620068	1	640456-4	74868
J5	3 Pin	2620121	1	640456-3	74868
P2	26 Pin, Right Angle	2620131	1	3493 - 1002	76381
Q1 thru Q15	PNP, Power	4710027	15	MPS - D54	04713
Q16	NPN, General Purpose	4704124	2	2N4124	04713
Q17	Q16				
R1	Comp, 10K, 5%, 1/4W	4010103	2	RC07GF103J	81349
R2	Comp, 220, 5%, 1/4W	4010221	1	RC07GF221J	81349
R3	Comp, 75K, 5%, 1/4W	4010753	1	RC07GF753J	81349
R4	Variable, Cer., 200K	4250022	1	72XR200	73138
R5	Comp, 120K, 5%, 1/4W	4010124	1	RC07GF124J	81349
R6	Comp, 2.4K, 5%, 1/4W	4010242	1	RC07GF242J	81349
R7 thru R21	Comp, 1K, 5%, 1/4W	4010102	15	RC07GF102J	81349
R22	Not Used				
R23	Comp, 15K, 5%, 1/4W	4010153	1	RC07GF153J	81349
R24	Comp, 390, 5%, 1/4W	4010391	1	RC07GF391J	81349
R25	Comp, 200, 5%, 1/4W	4010201	1	RC07GF201J	81349
R26	Comp, S.A.T 1K NOM , 1/4W, 5%	4010999	1		
R27	R1				
R28	Not Used				
R29	Comp, 2.2K, 5%, 1/4W	4010222	1	RC07GF222J	81349
R30	Not Used				
R31	Comp, 27K, 5%, 1/4W	4010273	1	RC07GF273J	81349
R32 thru R34	Comp, 39K, 5%, 1/4W	4010393	3	RC07GF393J	81349
RN1	Network, 10K	4170003	2	785-1-R10K	32997
RN2	RN1				
RN3	Network, 10K	4170004	1	784-1-R10K	32997

A111 FRONT PANEL DRIVER continued

2020191-02 A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
TP1 thru TP6	.040D Pin	2620032	9	460-2970-02-03	71279
TP7	Not Used				
TP8 thru TP10	TP1				
U1	TTL, Monostable, MV	3084123	2	DM74LS123N	0000X
U2	4-16 Line Decoder	3074154	1	DM74154N	0000X
U3	4 Bit Shift Register	3084195	1	DM74LS195N	0000X
U4	AND - OR - INVERT Gates	3087451	1	SN74LS51N	01295
U5	Quad, 2 INP NAND Gate	3084132	1	DM74LS132N	0000X
U6	Binary Sync Clear	3084163	1	SN74LS163	01295
U7	Bipolar RAMS	3057489	2	DM74LS189	0000X
U8	U7				
U9	Oct Bus Trans	3084244	1	SN74LS244N	01295
U10	U1				
U11	Periph, Interface Adaptor	3086821	1	MC68B21P	04713
U12	Hex Inverter	3087414	1	SN74LS14N	01295
U13	8INP NAND Gates	3087430	1	DM74LS30N	0000X

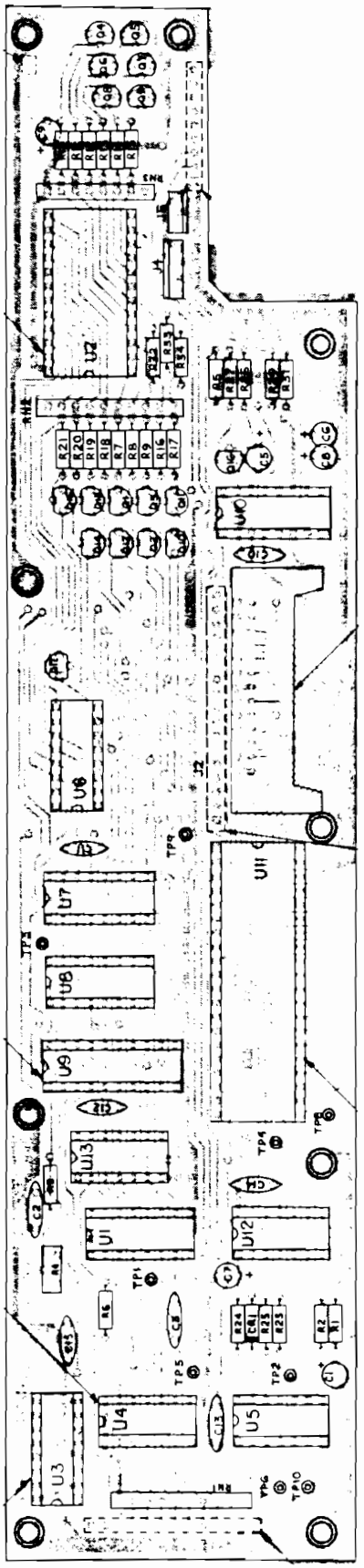

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Figure 111-3 Front Panel Component Locator

A203
BAND 3 MICROWAVE CONVERTER

The A203 Microwave Converter consists of three sub-assemblies:

- A201A Voltage Control Oscillator
- A201B IF Amplifier
- A202 Microwave (YIG)

CAUTION

Disassembly of the A202 Microwave assembly, or removal of it from the A201A VCO or A201B IF Amplifier will void the EIP warranty.

The assembly drawing and schematic for both the VCO and IF circuits are not available. The entire A203 assembly must be tested as a complete unit to ensure proper performance of the counter. Repair of the A202 Microwave assembly can only be done at the factory. The VCO and IF Amplifier boards require special test equipment, therefore field repair is not recommended.

The Band 3 Converter is a complete microwave subsystem (see Figure 203-1) which converts an input signal in the 1 to 20 (26.5) GHz range down to an IF of 127 MHz. Down conversion is achieved in this heterodyne system by combining the input signal with a harmonic of a precisely known reference signal (F_{VCO}). The mixer then produces a signal (F_{IF}) equal to the difference between the input and reference harmonic. If this difference is close to 127 MHz, it is amplified to a level of about 0 dBm and then counted. The input signal is then determined from the equation $F_{IN} = NF_{VCO} + F_{IF}$. F_{VCO} is set by the instrument program via a phase locked loop located on the converter control board (A108) and is thus known exactly. harmonics of the VCO are produced by the comb generator and coupled to the mixer. The frequency ranges of the VCO and IF are such that for any VCO frequency and any input frequency, only one harmonic can produce an IF frequency. The YIG filter located between the RF input and the mixer is used to approximately determine the input frequency and from this information the desired values of N, F_{VCO} and +/- are determined.

Two other outputs are obtained from the Band 3 Converter. The first is an analog signal which is a measure of input RF power. The second is a digital signal ($\overline{\text{IF THRESHOLD}}$) which indicates that an IF signal exists at a level of -3 dBm or greater.

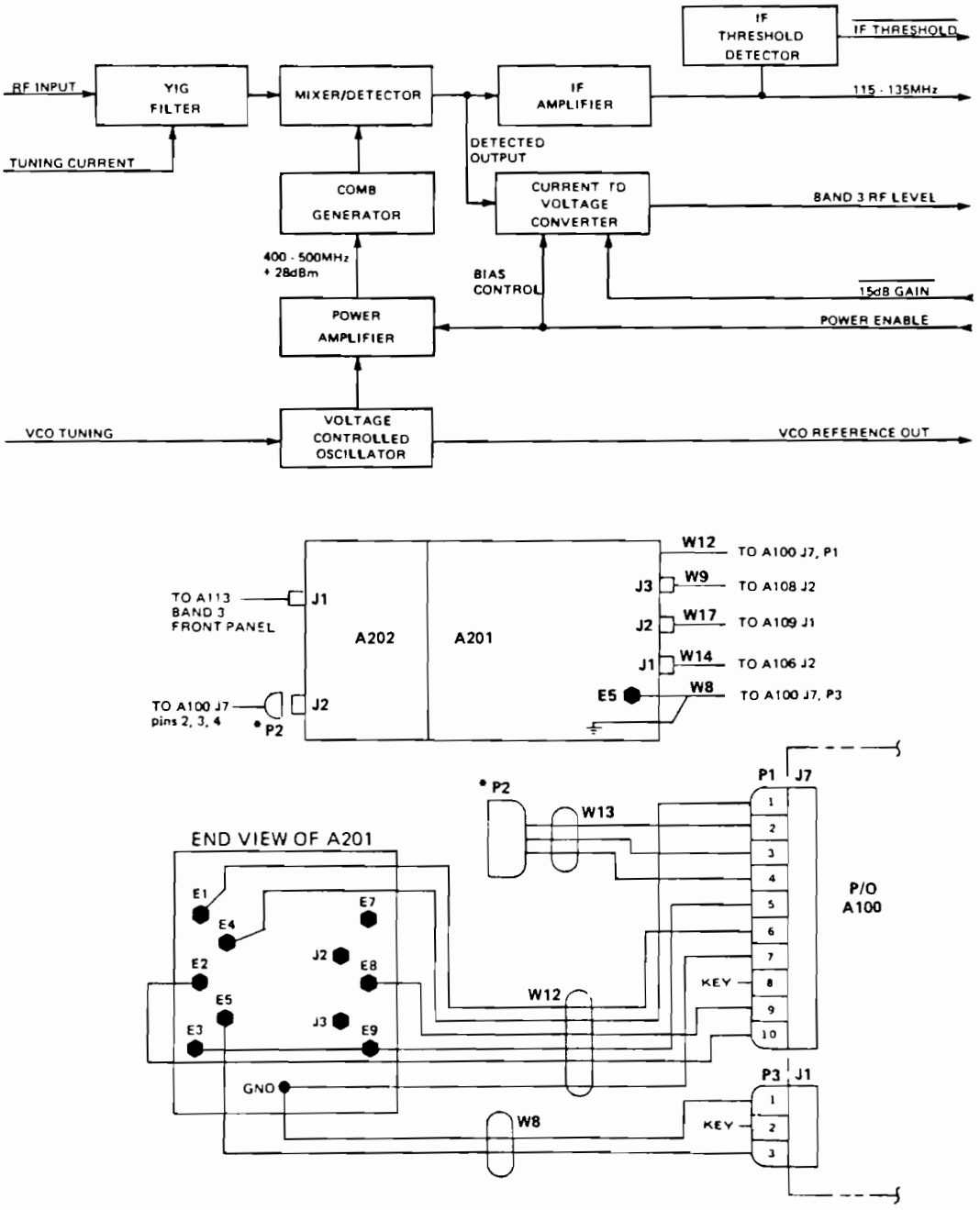


Figure 203-1. Band 3 Microwave Converter Diagram

Section 10
Options

Section 10 provides descriptions, specifications (where applicable), schematic diagrams and component locators for the options available for use with the Model 535B or 538B counter.

OPTION	
01	
02	
03	TIME BASE OSCILLATOR <5 X 10^{-9} (2010143-03)
04	TIME BASE OSCILLATOR <1 X 10^{-9} (2010143-04)
05	TIME BASE OSCILLATOR <5 X 10^{-10} (2010143-05)
06	
07	
08	GENERAL PURPOSE INTERFACE BUS (GPIB)
09	REAR PANEL INPUT
10	CHASSIS SLIDES
12	+5 DB SENSITIVITY
13	MATE-CIIL INTERFACE

OPTIONS 03, 04, 05
TIME BASE OSCILLATORS

Three Time Base Oscillators are available as options for either the model 535B or 538B. These high stability options enhance the accuracy of the counter by the addition of oven stabilizied crystal oscillators. These oscillators improve counter operation by reducing both time and temperature variations.

When any one of these options is installed, the TCXO is removed from the Gate Generator board (A107) and the following components are added.

- One of three Oven Oscillators (A114) mounted on the chassis.
- 28 VDC Power Supply board (A112), assembly part number 2010226.
- Power Supply Transformer T1 (part number 4900006) mounted on A112.
- Time Base Adjustment Pot J2 (part number 2010190) mounted on the rear panel.
- Related interconnecting cable harnesses.

	OPTION 03	OPTION 04	OPTION 05
CHARACTERISTIC	2030010-01	2030010-02	2030010-03
AGING RATE/24 HOURS (After 72 hour warm-up)	$< \mid 5 \times 10^{-9} \mid$	$< \mid 5 \times 10^{-9} \mid$	$< \mid 5 \times 10^{-10} \mid$
SHORT TERM STABILITY (1 second average)	$< 1 \times 10^{-11}$ rms	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms
0° to + 50° C TEMPERATURE STABILITY	$< \mid 6 \times 10^{-8} \mid$	$< \mid 3 \times 10^{-8} \mid$	$< \mid 3 \times 10^{-8} \mid$
± 10% LINE VOLTAGE CHANGE	$< \mid 5 \times 10^{-10} \mid$	$< \mid 2 \times 10^{-10} \mid$	$< \mid 2 \times 10^{-10} \mid$

Figure 03/04/05-1. Time Base Oscillator Option Specifications

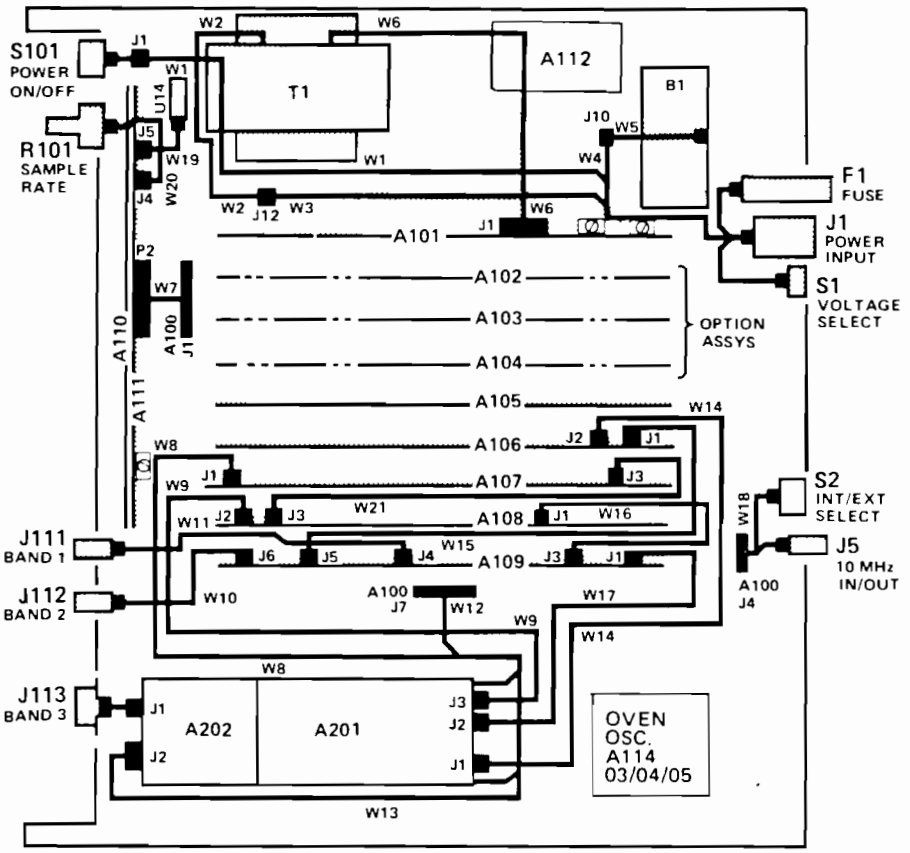


Figure 03/04/05-2. Component Location, Time Base Option

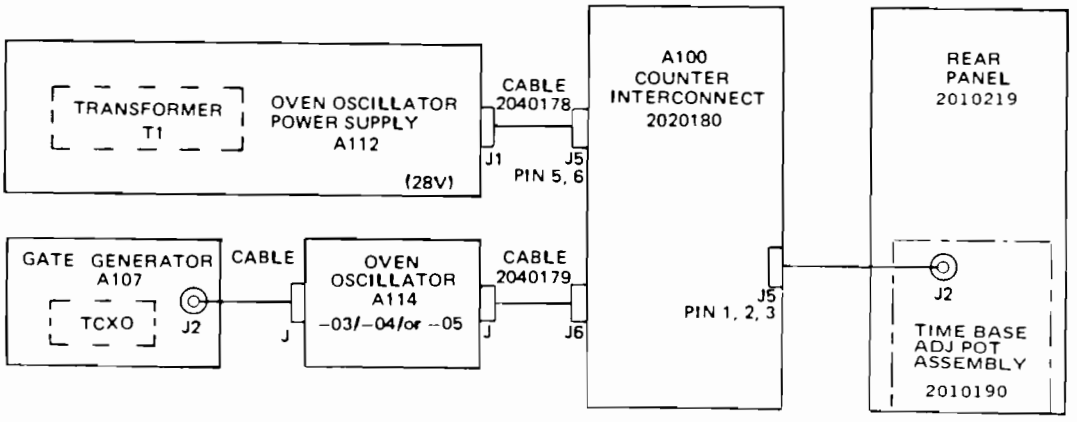


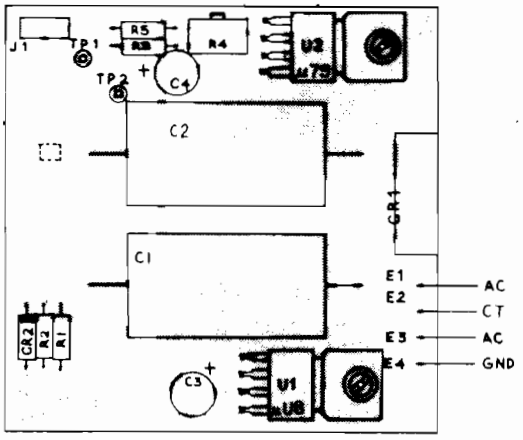
Figure 03/04/05-3. Time Base Option, Interconnection Diagram

OVEN OSCILLATOR POWER SUPPLY

The Oven Oscillator Power Supply board (A112) is a simple 28V regulated, current limited power supply. U1 and U2 provide voltage regulation, thermal protection and current limiting.

The transformer T1, CR1, C1 and C2 provide a 40V nominal unregulated DC voltage. The output voltage is set by voltage divider R5, R3 and R4. These resistors were selected so that 28V out provides 2.23V at U2 pin 2 (to U2 pin 1). Diode CR2 protects the supply from being pulled more negative than ground. See the schematic in figure 03/04/05-6.

The power supply (A112) is on and operating as long as the counter is connected to an active AC power source. The counter's POWER ON/OFF switch on the front panel does not control this assembly.



2020186 B

Figure 03/04/05-4. Oven Oscillator Power Supply (A112) Component Locator

OVEN OSCILLATOR CALIBRATION

When options 03, 04 or 05 are installed in the counter, the effects of temperature perturbations and aging must still be considered, although the magnitude of the inaccuracies associated with each oscillator are greatly reduced.

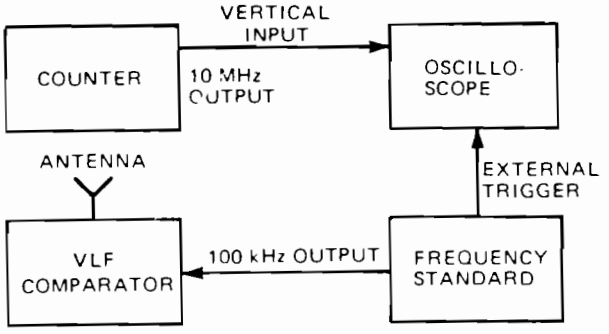
Full benefit of the oven stabilized oscillator characteristics can only be realized if the oscillator is running continuously (with counter always connected to a source of AC power). Under these conditions the perturbations in frequency will generally be in the positive direction for either an increase or decrease in temperature from + 25° C. The aging characteristic is also generally in the positive direction.

How frequently the oscillator is adjusted is determined by the level of accuracy required. To adjust the oscillator to an inaccuracy of less than 1×10^{-9} parts, relative to a standard, use this procedure. The test is illustrated in figure 03/04/05 - 5.

Observe the drift of the oscilloscope pattern. The fractional frequency offset is computed from:

$$\frac{T_{\text{drift of zero crossing}}}{T_{\text{observation time of drift}}} = \frac{\Delta f}{f}$$

If the pattern drifts at a rate of .01 microsecond every 10 seconds, the frequency is in error by 1 part in 10^9.



OVEN OSCILLATOR A114

Figure 03/04/05-5. Time Base Calibration.

All frequency checks and adjustments should be made only after the oscillator has been connected to its power source for 24 hours. If the oscillator has been disconnected from its power source for more than 24 hours it may require 72 hours of continuous operation to achieve the specified frequency aging rate.

To measure oscillator frequency:

1. Connect the counter's internal oscillator output signal from the 10 MHz IN/OUT connector (on the rear panel of the counter) to the vertical input of the oscilloscope.

2. Trigger oscilloscope externally with the frequency standard. The VLF Comparator is used to determine the absolute frequency of the standard.

3. Set oscilloscope sweep rate to 0.1 μ sec/cm and expand X10; this results in a sweep rate of .01 μ sec/cm.

4. Adjust oscilloscope vertical controls for maximum gain.

5. Determine the frequency difference (see page 6-24).

6. Horizontal drift of oscilloscope display in μ sec/sec, is a measure of the difference between the frequency standard and the counter oscillator frequency. If the difference is excessive for the desired counter application, vary the TIME BASE ADJUST control on the rear panel of the counter until the pattern stops drifting.

NOTE

For highest accuracy, the counter should be operated for 72 hours prior to adjustment.

OPTION 03/04/05 - TIME BASE OSCILLATOR PCB ASSYs 2020186 - B

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A112	OSCILLATOR POWER SUPPLY	2020186	1	EIP	
C1	Elec, 680 uF, 40V	2200021	2	3074JH681T040JPB	80031
C2	C1				
C3	Tant, 10 uF, 25V	2300029	2	DF106M25S	NEC
C4	C3				
CR1	Bridge Rectifier	2710019	1	SBMB1	14099
CR2	Rectifier	2704001	1	IN4001	
R1	Met Ox, 3.3K, 2%	4130332	1	C4/2%/3.3K	24546
R2	Met Ox, 2K, 2%	4130202	1	C4/2%/2K	24646
R3	Met Ox, 560, 2%	4130561	1	C4/2%/560	24546
R4	Variable, Cer, 500, 10%	4250014	1	72XR500	73138
R5	Met Ox, 3.6K, 2%	4130362	1	C4/2%/3.6K	24546
U1	Positive Voltage Regulator	3040780	1	uA78MGUIC	07263
U2	Negative Voltage Regulator	3040790	1	uA79MGUIC	07263

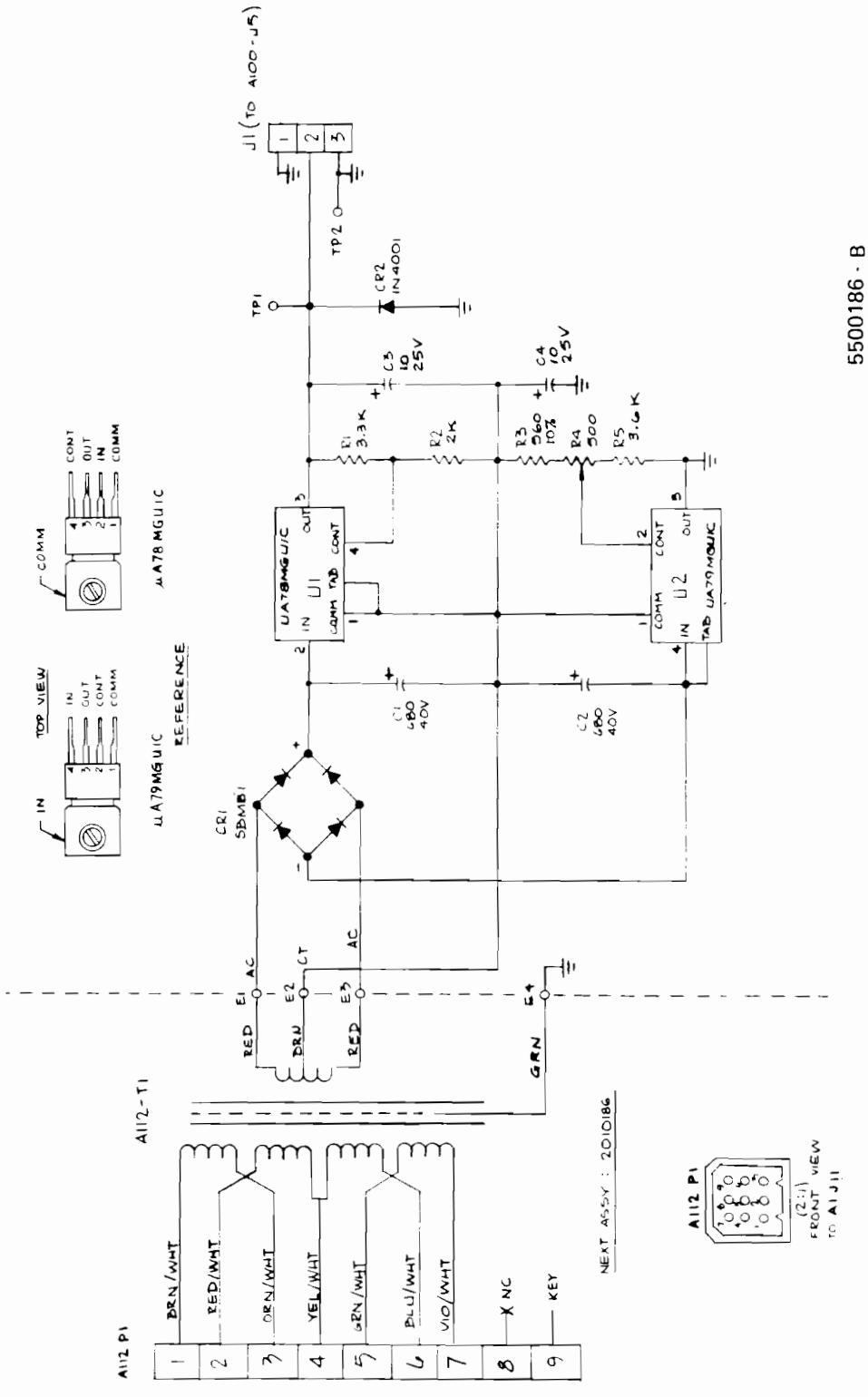


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Figure 03/04/05-6. Time Base Option Schematic

OPTION 06
EXTENDED FREQUENCY CAPABILITY

The frequency range extension option is available on the 538B counter. This option, when used with the model 590 Frequency Extension Cable Kit and the option 91 remote sensor, enables the counter to operate to 40 GHz. The option consists of:

- Band 4 Converter Module
- Band 4 Software
- Modified Front Panel Overlay
- Coax Cable, Front Panel to A204 J1 - P/N 2040232
- Coax Cable, Front Panel to A204 J2 - P/N 2040231

KEYBOARD OPERATION

To operate the counter in one of the Band 4 frequency ranges, connect the short cable (supplied with the frequency extension kit) from the lower output jack on the front panel, to the Band 3 input. Connect the long cable from the upper jack to the remote sensor.

NOTE

Before connecting the remote sensor to the frequency source, verify that the power level is within the limits specified for the sensor. When you connect the sensor the counter will automatically display the reading.

To select Band 4:

PRESS: [BAND] Band annunciator flashes

PRESS: [4] Band 4 annunciator flashes

SPECIFICATIONS

BAND	FREQUENCY RANGE	SENSITIVITY (TYPICAL)	MAX. INPUT	REMOTE SENSOR MODEL
41	26.5 - 40 GHz	{ -25 dBm typ. -20 dBm min. }	+5 dBm	91

GPIB OPERATION

To select Band 4 through the GPIB, input B4.

THEORY OF OPERATION - HARDWARE

When measuring a signal frequency greater than 26.5 GHz, the 538B using the Option 06 Frequency Extension with a model 590 kit and a 91 remote sensor down converts the input to approximately 1.0 GHz. This signal is then fed to the Band 3 input, where a second conversion produces 127 MHz IF.

a multiplier chain increases the VCO output frequency to the 5.28-6 GHz range, which is referenced to the time base. See Figure 06-1. This signal provides the local oscillator (LO) power, which is transmitted to the remote sensor, an external harmonic mixer. When the input frequency and harmonics of the LO, (generated in the mixer) combine, a first IF is generated in the range of 1.00-1.35 GHz.

A diplexer separates the LO and IF signals received from the harmonics mixer. The level of the IF is then increased to a minimum of -25 dBm via the IF amplifier, then supplied to the Band 3 converter input.

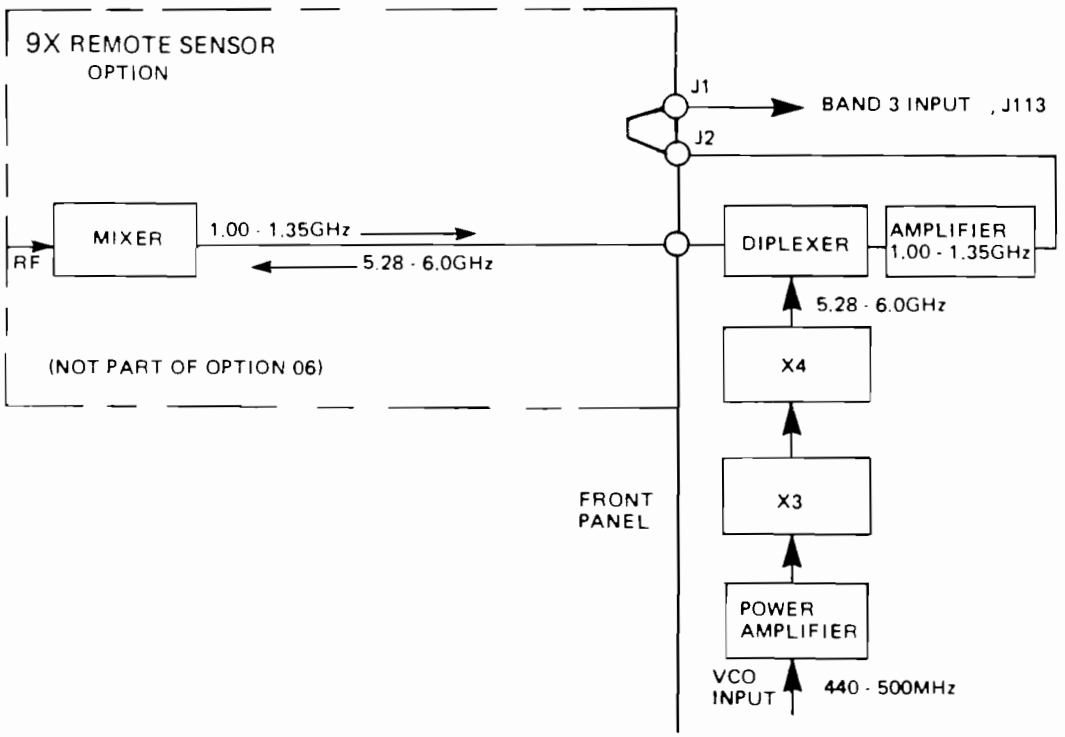


Figure 06-1. Frequency Extension Block Diagram

THEORY OF OPERATION - SOFTWARE (LOCKING ROUTINE)

The Band 4 software performs two main functions: it locks onto an incoming RF signal, and it tracks an RF signal once it is locked.

The locking routine is called by the supervisor when any of the following conditions are met:

1. Selection of Band 4
2. Software called from the source lock routine.
3. Loss of IF threshold after being locked.
4. Any reset condition.

LOCKING PROCESS

Initialization

The initialization routine clears the working table (BANDTB) for Band 4 and loads from PROM the table of constants that is used by the program for the selected Band 4 subband. BANDTB is an area in RAM that is 40 bytes long.

VCO Sweep

This routine steps the VCO frequency by a step size stored in BANDTB. After each step, it checks the VCO frequency for three stop points.

1. Top VCO frequency limit (depends on subband),
2. Wraparound frequency
3. Lockout frequency

If the top VCO frequency has been reached and no signal has been found, the program returns to the supervisor. If the top frequency is reached, and a signal has been detected, the VCO is set to its low limit and the bottom range is searched until the wraparound frequency is reached.

If the wraparound frequency has been reached (the frequency at which the last VCO frequency has produced the strongest IF signal), then the program stays at this frequency, and performs the centering and harmonic number calculation routines.

If a lockout frequency (a VCO frequency at which erroneous locking results) is detected, the VCO frequency will be incremented by :

8 * step size = new VCO frequency

and the program continues from this frequency.

After each VCO step, the YIG filter is swept to see if a signal is detected by the power DAC attenuator. If a signal is detected, the YIG is swept back and forth, and the attenuation is increased until the signal is lost. At this point a new VCO frequency is stepped and the process of signal detection continues and the power DAC is left at the last setting to detect the next highest signal.

Centering and Harmonic Numbering Determination

After the VCO sweep routine is complete and the VCO frequency is set, the incoming signal is mixed with a harmonic of the VCO frequency to produce a signal in a predetermined passband region (1.05 GHz to 1.25 GHz). Then a small VCO frequency is incremented to determine the mix side. After the VCO step, if the resulting IF increases, it is high side mix, otherwise, it is low side mix. The IF is then stepped to 1.05 GHz (or as close as possible) by using the following formula to calculate the VCO step size:

$$\frac{(\text{IF} - 1050\ \text{MHz}) * 100}{12 * \text{N\_MAX}}$$

Where N_MAX is the highest harmonic number allowed in the subband.

The above calculation is performed at most twice to bring the IF to 1.05 GHz. At this point the YIG is centered and the centering frequency FYIG1 and VCO frequency FVCO1 are stored. Next the VCO is stepped to bring the IF to around 1.25 GHz and a new centering takes place. This second center frequency is stored for later calculation of the harmonic number. Next the signal is stepped to its previous position and centered. This center frequency is now compared to FYIG1, and must be within 6 MHz. If it is not within 6 MHz, it is assumed that the signal is moving, and the Band 4 program exited.

The IF frequency step size, caused by the VCO frequency step, is used to determine the harmonic number by the following equation.

$$\frac{\Delta \text{ IF FREQ. DUE TO VCO STEP}}{\text{HARMONIC SPACING}} = \text{HARMONIC \#(N)}$$

Where harmonic spacing = VCO step size X 12

CALCULATION ROUTINE – The calculation routine is used to find the approximate RF frequency F_{IN} in the following manner.

1. Compute $F' = 12\ N\ X\ F_{VCO}$
2. Center the YIG filter on the first IF
3. Convert the binary YIG frequency to BCD
4. Compute $F_{IN} = F' \pm F_{YIG}$ (where F_{YIG} gives the approximate value for the first IF).
5. Compute a corrected VCO frequency using the equation:

$$F_{VCO} = (F_{IN} \pm 127) / (12N \pm 2)$$

Then tune the VCO with the corrected frequency and center the first IF frequency in the YIG passband

SHALLOW SEARCH – This routine tests for a signal in the IF passband. If a signal is present, the routine is exited. If a signal is not present, the routine will search an RF range of ±60 MHz (in steps of 200 kHz), for the signal, and continues if a signal is found. If a signal is not found, the Band 4 program returns control to the supervisor.

BAND 4 TRACKING – The tracking routine centers the second IF in the following range.

$$115\ \text{MHz} < \text{2nd IF SIGNAL} < 135\ \text{MHz}$$

This routine is called from outside of the Band 4 program to track a signal. A test is first made to determine if an IF threshold is present. If IF threshold is present it continues, if not the program returns to the supervisor to start the locking process from the beginning.

This routine reads the second IF frequency and computes the new VCO frequency so that the second IF is in the range given above. A new YIG frequency is calculated and the VCO and YIG are "tuned" to produce a new IF. A new FLO (frequency added to the second IF to produce the displayed frequency), is calculated. The equation for this process is:

$$F_{LO} = F_{VCO}\ (12\ N \pm 2)$$

The YIG frequency is: NEW F_{YIG} = 2 (NEW VCO) + 127 MHz.

PERFORMANCE TESTS

The Band 4 converter module is not field repairable. When a malfunction is suspected, its operation can be checked from the front panel as follows:

IF AMPLIFIER — Apply a -50 dBm signal to the diplexer port (upper output jack) from 1.0 to 1.35 GHz. Output should be greater than -13dBm as checked on a spectrum analyzer to the IF output (lower jack).

LO SIGNAL — Connect a spectrum analyzer to the diplexer port (upper output jack). Using the following formula, set the VCO frequency between 440 and 500 MHz. The spectrum analyzer should show the 12th harmonic of the VCO frequency (5.28-6 GHz). The spectrum analyzer signal should be +8 dBm minimum, and free of breakup and spurious signals to -30 dBc.

To convert from the desired VCO frequency to the PIA program number:

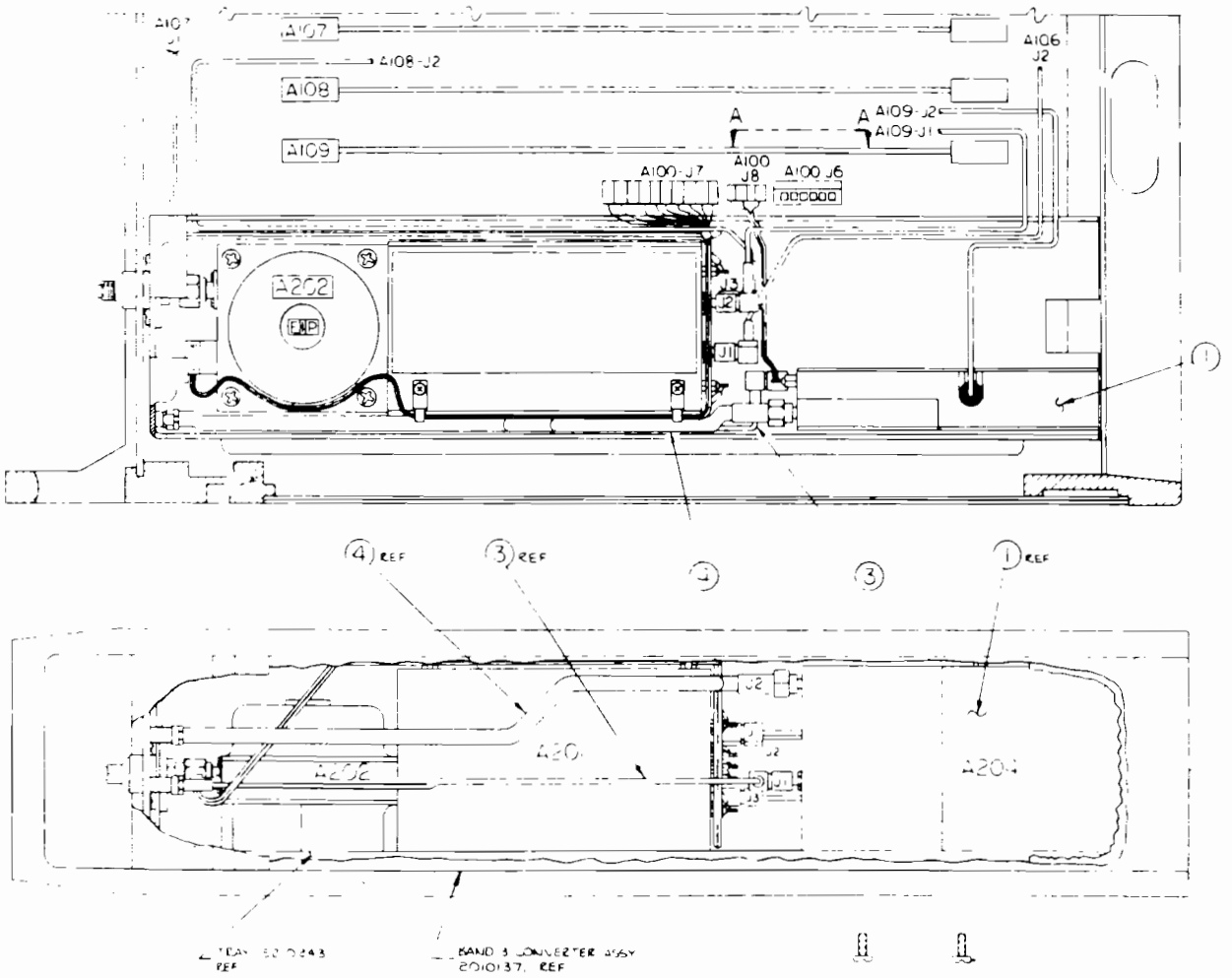
EXAMPLE (440.75 MHz)

1. Round the desired frequency to a multiple of 50 KHz (The resolution of the VCO frequency is 50 KHz).
2. Multiply the desired frequency (in MHz) by 5 . . . . . 440.75 X 5 = 2203.75
3. If the result contains no fractional part, go to step 8.
4. Multiply only the fractional part by 16 . . . . . .75 x 16 = 12
5. Add the result to the most significant digit from step 2 . . . . . MSD of 2203.75 = 2 — 2 + 12 = 14
6. Convert the result to hexadecimal . . . . . $14_{10} = E_{16}$
7. Replace the MSD from step 2 with the result from step 6 and drop the fractional part . . . . . 2203.75 → E203
8. The two most significant digits are programmed to address 1822, and the two least significant digits are programmed to address 1820.

To remove a defective converter:

1. Remove the line cord and both the top and bottom cover of the counter.
2. Remove the two screws holding the converter in place from the bottom.
3. Remove coaxial cables and unplug DC harness.
4. Lift the converter out of the counter.

To replace, proceed in the reverse order.



① Band 4 Converter – 2010229

③ Cable (FP to A204J1) – 2040232-01

④ Cable (FP to A204J2) – 2040231-01

Figure 06-2. Location of Installed Band 4 Converter (A204)

OPTION 08

GENERAL PURPOSE INTERFACE BUS

Option 08 makes 535/538 microwave counters fully compatible with the General Purpose Interface Bus (GPIB). With this option the counter can respond to remote control instructions and can output measurement results via the IEEE 488-1978 Bus interface. At the simplest level the counter can output data to other devices such as the HP 5150A Thermal Printer. In more sophisticated systems a calculator or other system controller can remotely program the counter, trigger measurements, and read results. Of course, a calculator or computer adds other benefits to a GPIB based measurement system. The calculator can manipulate data to compute the mean and standard deviation, check for linearity, and compare results to limits, or perform many other functions.

GPIB FUNCTIONS IMPLEMENTED

The GPIB interface function subsets implemented are:

SH1	complete capability
AH1	complete capability
T5	basic talker, serial poll, Talk Only mode, unaddress if MLA
L3	basic listener, Listen Only mode, unaddress if MTA
SR1	complete capability
RL1	complete capability
DC1	complete capability
DT1	complete capability

NOTE

When DEVICE CLEAR or SELECTED DEVICE CLEAR GPIB bus command is received, the counter will revert to the power on state. When DEVICE TRIGGER GPIB bus command is received, the counter will initiate a new frequency reading cycle. The converter will not be reset. When counter is in REMOTE the RESET key, on the front panel keyboard, acts as the RETURN to LOCAL key.

SETTING ADDRESS SWITCH

The counter employs a decimal address switch located on the top edge of A102. It is set for decimal address 19 at the factory. To verify the switch setting without removing the top of the counter, simply initiate test 10; enter 9C04 and read the address on the display. A description of test 10 can be found on page 6-7. After reading the address, terminate the test by pushing the clear display key.

The address switch is also used to put the counter in the Talk Only (TO) or Listen Only (LO) mode. To put the counter in the Listen Only mode simply set the address switch to any number from 41 to 99.

The counter can be put in four different modes of operation in the Talk Only mode. The following is a list of the address settings for entering these modes.

ADDRESS	MODE OF OPERATION
32	Continuous output determined by SAMPLE RATE control. Exponent in scientific format.
33	Continuous output - fast active. SAMPLE RATE control inactive. Exponent in scientific format.
34	Continuous output determined by SAMPLE RATE control. Exponent in zero output format.
35	Continuous output - fast active. SAMPLE RATE control inactive. Exponent in zero output format.

NOTE

In the Talk Only or the Listen Only mode, the address of the counter is always automatically set to decimal 0.

DEVICE DEPENDENT DATA INPUT

It takes a specific amount of time for the counter to process the input data (error checking, formatting, changing the mode of operation, etc.). To prevent the data rate of the bus from slowing down while the counter is doing input data processing, the data is accepted as soon as it is available on the bus, and it is temporarily stored in memory. The size of the storage memory is 100 characters.

The users of the GPIB option need to be aware that there is a difference between accepting data and complying with it. If the counter is asked to output a reading before it has finished processing the input data, the output will be in error if the operator makes the assumption that the counter is in the mode that was just programmed. To prevent this, sufficient programmed delays must be provided, or use must be made of the counter's Service Request status byte. See Service Request (SR) command description.

GPIB INSTRUCTION FORMAT

<OP CODE> <NUMBER> <TERMINATOR>

OPERATION CODE or OP CODE can take any of the following formats:

<LETTER> <LETTER> or <LETTER> <DIGIT>

Example: FH (Frequency limit high) or B3 (band 3)

The NUMBER portion of the statement can take the form of any of the following:

<SIGN> <DIGIT STRING>

Example: –2457

<SIGN> <DIGIT STRING> • <DIGIT STRING>

Example: –3.483

NOTE: Spaces within the <OP CODE> and <NUMBER> portions of the instructions are always ignored.

The TERMINATOR allows the operator to choose the scale of an input number as well as implement special functions.

TERMINATOR = G/M/K/H/D/P/C

G, M, K, H, represent GHz, MHz, kHz and Hz respectively
D = dB, P = clear data, (equivalent to "clear data" key on keyboard)
C = clear display (equivalent to "clear display" key on keyboard)

FORMAL DEFINITION OF INSTRUCTIONS

<OP CODE> <NUMBER> <TERMINATOR>

<OP CODE> :: = <LETTER> <LETTER> | <LETTER> <DIGIT>

<NUMBER> :: = <SIGN> <DIGIT STRING> |
<SIGN> <DIGIT STRING> . <DIGIT STRING> |
NULL

<TERMINATOR> :: = G | M | K | H | D | P | C | NULL

<SIGN> :: = + | − | NULL

<DIGIT STRING> :: <DIGIT> <DIGIT> <DIGIT> · · · · · · ·

<LETTER> :: = A | B | C | D | E | F | G | H | I | J | K | L | M | N |
O | P | Q | R | S | T | U | V | W | X | Y | Z

<DIGIT> :: = 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 0

PROGRAM CODE SET

Codes underlined indicate start-up conditions. These conditions are set by the device clear or selected device clear, or power on.

DISPLAY

DA – Display Active: Output Frequency Reading to Front Panel and Bus
DP – Display Passive: Output Frequency Reading to Bus only
DN – Display Normal

BAND

B1 – Band 1: 10Hz - 100MHz
B2 – Band 2: 10MHz - 1GHz
B3 – Band 3: 1GHz - 18GHz (26.5 GHz)

RESOLUTION

R0 – Resolution 0 = 1Hz
R1 – Resolution 1 = 10Hz
R2 – Resolution 2 = 100Hz
R3 – Resolution 3 = 1KHz
R4 – Resolution 4 = 10KHz
R5 – Resolution 5 = 100KHz
R6 – Resolution 6 = 1MHz
R7 – Resolution 7 = 10MHz
R8 – Resolution 8 = 100MHz
R9 – Resolution 9 = 1GHz

MEASUREMENT FUNCTIONS

FA – Fast Active (Ignore sample rate Pot)
FP – Fast Passive (Terminates FA)
RS – Reset Basic Counter and Converter. Take a new reading after reset.
HA – Hold Active
HP – Hold Passive

DATA MANIPULATION FUNCTIONS

FO – Frequency Offset. Take a new reading after data entry if counter not in hold.

*OA – Offset Active:
–Add Frequency Offset to Frequency Reading

OP – Offset Passive (Terminates OA)
ML – Multiplier. Multiplies frequency readings by an integer number.

*In Start-up Condition, although OA is Active, "0" (zero) Frequency and Power Offsets are programmed.

SELF-TEST FUNCTIONS

TA – Test Active.
TP – Test Passive. (clear test function)

DATA FORMAT

EZ – Exponent Zero
ES – Exponent Scientific

DATA OUTPUT

FR – Output frequency readings only

SERVICE REQUEST

SR – Service request enable

DESCRIPTION OF AVAILABLE COMMANDS

DISPLAY

DA - Display Active - Outputs readings to both front panel and GPIB bus

DP – Display Passive - Outputs readings to GPIB bus only. It will decrease the cycle time of the counter.

DN – Display Normal - Resets display only; used for clearing error messages on the display. Cannot be used after verifying preprogrammed data such as Frequency Offsets or Frequency Limits. This OPCODE affects only the display.

BAND

B1 – Selects Band 1

B2 – Selects Band 2

B3 – Selects Band 3

RESOLUTION

R0 thru
R9 – Resolution 0 thru 9 - Picks the front panel resolution from 1Hz to 1GHz. Also chooses gate time which is related to resolution: 1Hz = 1 Sec, 10Hz = 100 Sec. 100Hz = 10 msec. 1kHz to 1GHz = 1 msec.

MEASUREMENT FUNCTIONS

FA – Fast Active - Causes the counter to go into the fast cycle mode of operation. In this mode, the front panel sample rate/hold control is inactive and the fastest sample rate is attained. The counter will not go into the Fast Active mode of operation until Hold Active is disabled.

FP – Fast Passive - Terminates FA.

RS – Reset Basic Counter and Converter - Re-acquires input signal and takes a new reading. Has the same function as manual reset button.

HA – Hold Active - The counter stops taking readings and the last frequency and power readings are displayed and held. The counter can be directed to take one reading when it is in this mode by sending Device Trigger or Selected Device Trigger GPIB bus command to the counter. It will also update the reading if the RS mnemonic is received.

HP – Hold Passive - Terminates HA.

DATA MANIPULATION FUNCTIONS

FO – Frequency Offset - Enables entry of frequency offsets. (1 Hz resolution available.) A new gate will be initiated after data entry if counter is not in HOLD.

OA – Offset Active - Add frequency offset to frequency readings. Add power offset to power readings if power meter function is active.

OP – Offset Passive - Does not add frequency and power offset to readings.

ML – Multiplier - Enables entry of a 2-digit frequency readings multiplier. The multiplier must be an integer between 00 and 99. The results are to 1kHz resolution. A new reading will be initiated after the data entry if the counter is not in HOLD. If the results of the multiplications are larger than, or equal to 999.999999999GHz, the counter will output 999.999999999GHz to the bus if asked to output readings.

SELF-TEST FUNCTIONS

TA – Test Active - Enables the counter to perform the selected test function by entering the mnemonic TA followed by two digits. When Test 05 or Test 10 is active and the counter is being asked to output data, the data that is displayed on the front panel is the data being output.

The output data format is as follows:

XXXXXXXXXXXXCRLF

X = alpha-numeric
CR = carriage return
LF = line feed

For detailed descriptions of Test 01 through Test 07, see the section on Keyboard Controlled Circuit Tests, page 6 6.

Test 10 operates in the following manner:

1. To activate Test 10 input TA10.
2. To read the data stored in a specific memory location, input the address of the memory location in a four digit hexadecimal number. Enable the counter to talk and then read data from the counter.
3. To alter the data stored in a certain memory location:

   If 2. has been performed - input the desired data for that memory location.

   If 2. has not been performed - input the memory address, followed by a two digit hexadecimal number.

TP – Test Passive - Terminates test function.

DATA FORMAT

EZ – Exponent Zero - output format.

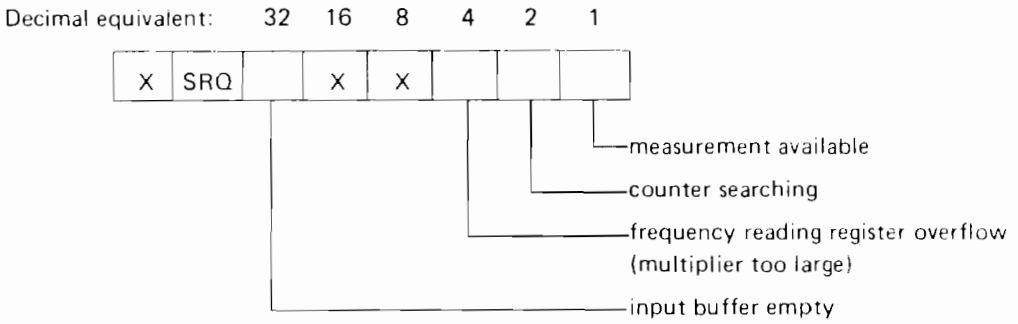
ES – Exponent Scientific - output format.

DATA OUTPUT

FR – Output frequency readings. (See section on output data format.)

SERVICE REQUEST

SR – Service Request Enable - Enables the counter to send Service Request to the bus when a certain event has taken place in the counter. To enable the function, input SR followed by two decimal digits. The two digits are the decimal equivalent of the content of the eight bit status register. More than one bit of the status register can be set.



To disable the Service Request function, input SR00.

NOTE

Even when the Service Request function is disabled, the Service Request status byte will still be continuously altered to reflect the internal states of the counter.

EXAMPLE: To enable service request on measurement available or input buffer empty, send SR33.

DATA OUTPUT FORMAT

The Model 535 transmits the following string of characters to output a measurement.

Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Format																		
EZ (Exponent Zero)	↛	±	D	D	D	D	D	D	D	D	D	D	D	D	E	0	CR	LF
ES (Exponent SCI)*	±	D	D	D	D	D	D	D	D	D	D	D	D	D	E	D	CR	LF

When the counter is in Test 05 or Test 10, the output will reflect the data on the display. The format is as follows:

XXXXXXXXXXXXCRLF.

↛ = Blank
D = Digit
X = Alpha-numeric
CR = Carriage Return
LF = Line Feed

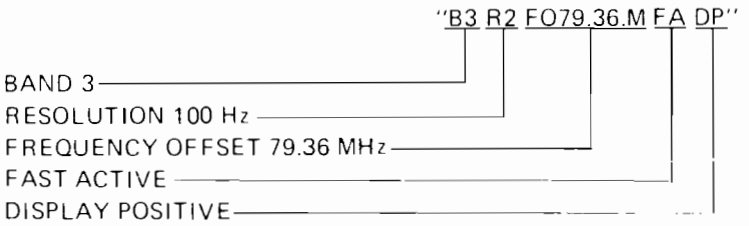
*in Exponent Scientific one digit represents the position of the decimal point. Exponent digit can be either 0, 3, 6, or 9.

Under different output modes, the following counter outputs can be expected by a listener.

OUTPUT MODE	COUNTER OPERATING MODE	OUTPUT
FR	PA	FREQ
	PP	FREQ
	TA01	FREQ

PROGRAM EXAMPLES

The examples given here assume an address setting of decimal 19 or ASCII talk address "S" and listen address "3" for the counter. By addressing the counter to listen and sending the following program string, it sets up the following measurement conditions.



The following programs illustrate how controllers function with the counter. These programs cause the counter to make a series of frequency measurements. The calculators read the measurements into memory and print the results. The programs assume the counter Talk and Listen address is decimal "19."

```
HP 9825A    0:  dim A (10)
            1:  rem 7
            2:  wrt 719, "B3R2FO-4.55M"
            3:  wait 300
            4:  for I = 1 to 10
            5:  red 719, A (I)
            6:  prt A (I)
            7:  next I
            8:  end
HP 9845A   10:  output 719, "B3R2FO-4.55M '
           15:  wait 300
           20:  input 719, A
           30:  print "Frequency minus offset equals," A
           40:  Go to 20
TED 4051   10:  print @19: "B3R2FO-4.55M"
           20:  input @ 19: A
           30:  print "Frequency minus offset equals," A
           40:  Go to 20
```

The 9825A program will cause the counter to take a series of ten readings, print them on the 9825A paper tape and stop. Notice that an offset of 4.55 MHz is subtracted from each reading.

The program shown for the 9845A and TEK 4051 cause the counter to make a frequency measurement and print that measurement. To end the program, initiate a "STOP" command. This is accomplished on the 9845A with the key labeled "STOP." On the TEK 4051 use the key labeled "BREAK." To restart the program enter the RUN statement followed by the line number that is printed in the INTERRUPT message.

READING A MEASUREMENT

To read a measurement from the counter to a calculator, the counter must first be addressed to talk and the calculator to listen. The examples below indicate how a calculator may read a measurement from the counter.

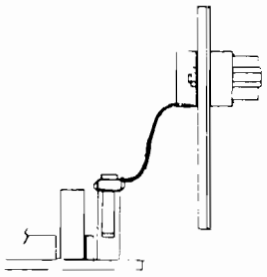
```
10 red 719, A
20 prt A                    } HP 9825A

10 input @ 19:A
20 print A                  } TEK 4051

10 enter 719, A
20 print A                  } HP 9845A
```

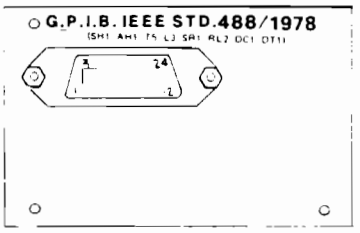
The EIP counters can use two different modes. HA takes one reading then waits for a reset command or a Device Trigger GPIB Bus Command. In this condition the counter is sent a reset or Device Trigger and (when addressed to talk) a new reading is output to the bus. The counter will hold that particular reading on the display until another reset command or Device Trigger command is received. The other mode is HP or HOLD PASSIVE. In this mode data is read out in a normal bus fashion. The display automatically updates corresponding to the sample rate chosen. In this condition successive readings can be output without generating a reset or Device Trigger command each time.

ADDRESS CHARACTERS		ADDRESS CODES					
Listen	Talk	binary					decimal
		5	4	3	2	1	*
SP	@	0	0	0	0	0	00
!	A	0	0	0	0	1	01
"	B	0	0	0	1	0	02
#	C	0	0	0	1	1	03
$	D	0	0	1	0	0	04
%	E	0	0	1	0	1	05
&	F	0	0	1	1	0	06
'	G	0	0	1	1	1	07
(	H	0	1	0	0	0	08
)	I	0	1	0	0	1	09
*	J	0	1	0	1	0	10
+	K	0	1	0	1	1	11
,	L	0	1	1	0	0	12
–	M	0	1	1	0	1	13
.	N	0	1	1	1	0	14
/	O	0	1	1	1	1	15
0	P	1	0	0	0	0	16
1	Q	1	0	0	0	1	17
2	R	1	0	0	1	0	18
3	S	1	0	0	1	1	19
4	T	1	0	1	0	0	20
5	U	1	0	1	0	1	21
6	V	1	0	1	1	0	22
7	W	1	0	1	1	1	23
8	X	1	1	0	0	0	24
9	Y	1	1	0	0	1	25
:	Z	1	1	0	1	0	26
;	[	1	1	0	1	1	27
<	/	1	1	1	0	0	28
=	]	1	1	1	0	1	29
>	^	1	1	1	1	0	30

* Decimal Talk/Listen Address is provided as a cross reference for those controllers which use decimal address.

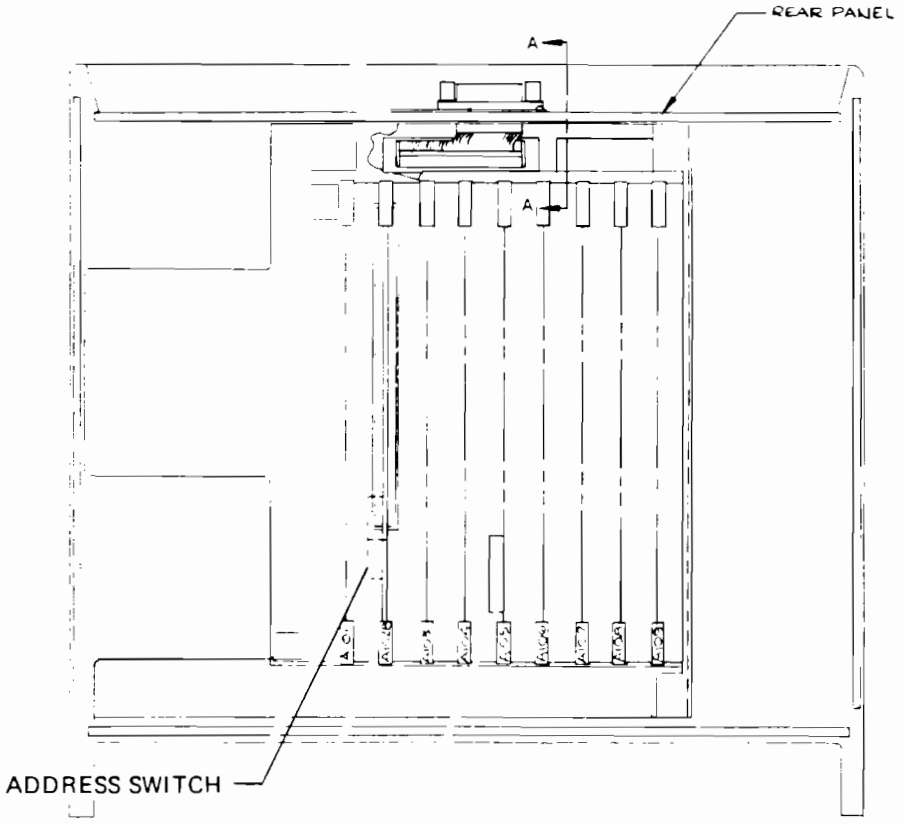
Figure 08-1. Allowable Address Codes





DETAIL A-A

CONTACT	SIGNAL LINE	CONTACT	SIGNAL LINE
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI	17	REN
6	DAV	18	GND (6)
7	NRFD	19	GND. (7)
8	NDAC	20	GND (8)
9	IFC	21	GND. (9)
10	SRQ	22	GND. (10)
11	ATN	23	GND (11)
12	SHIELD	24	GND LOGIC



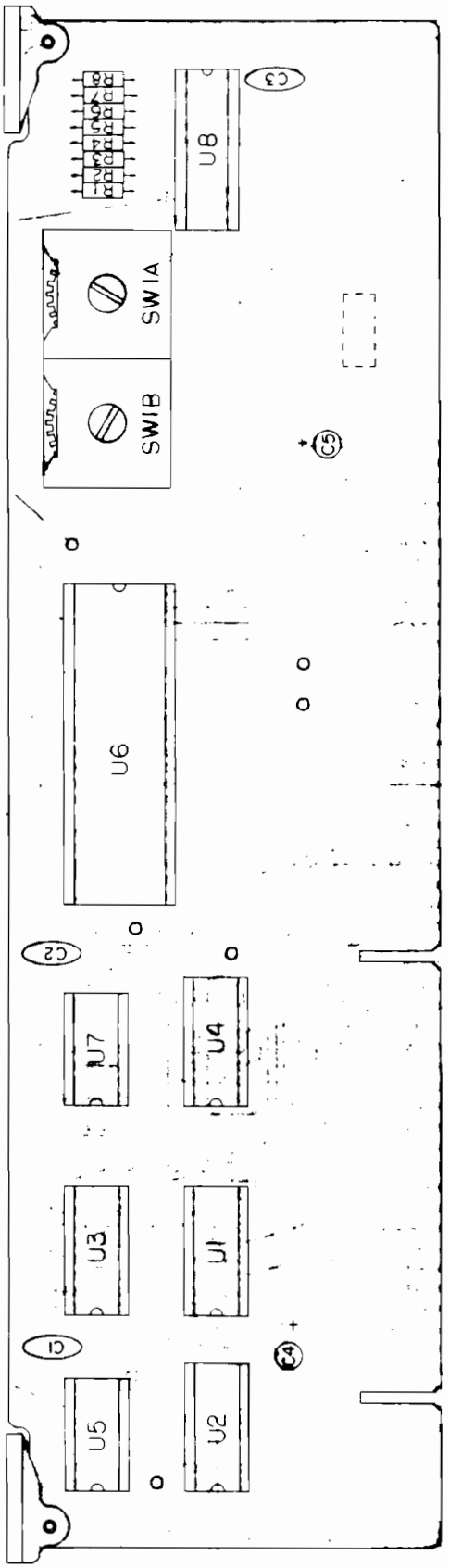
SEE G.P.I.B. MANUAL FOR ADDRESS SETTING INSTRUCTIONS.

Figure 08-2. Location of GPIB in Counter

OPTION 08---GENERAL PURPOSE INTERFACE BUS

2020133-02 A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO
08	GPIB Option	2010635-01		EIP	34257
-1	PCB Assy, GPIB (A102B)	2020133	1	EIP	34257
C1	Cer, .01μF, 20%, 100V	2150003	3	TG-S10	56289
C2	C1				
C3	C1				
C4	Tant, 33μF, 20%, 10V	2300015	2	TAG20-33/10-50	14433
C5	C4				
R1 thru R8	Comp, 5.6K, 5%, 1/4W	4010562	8	RC07GF562J	81349
SW1A and SW1B	Thumbwheel Switch	4540004	2	1X2270-0000	
TP1 thru TP6	P.C. pin .040 diameter	2620032	6	460-2970-02-03	71279
U1 thru U4	Quad 3 state Bus Transciever	3053448	4	MC3448	04713
U5	Hex Inverter	3087404	1	74LS04	27014
U6	General Purpose Interface Adaptor	3058488	1	MC68488	04713
U7	Tri Input NAND Gate	3087410	1	74LS10	27014
U8	Oct Bus Transciever	3084245	1	74LS245	27014



2020133-02 A

Figure 08-3. GPIB Component Locator

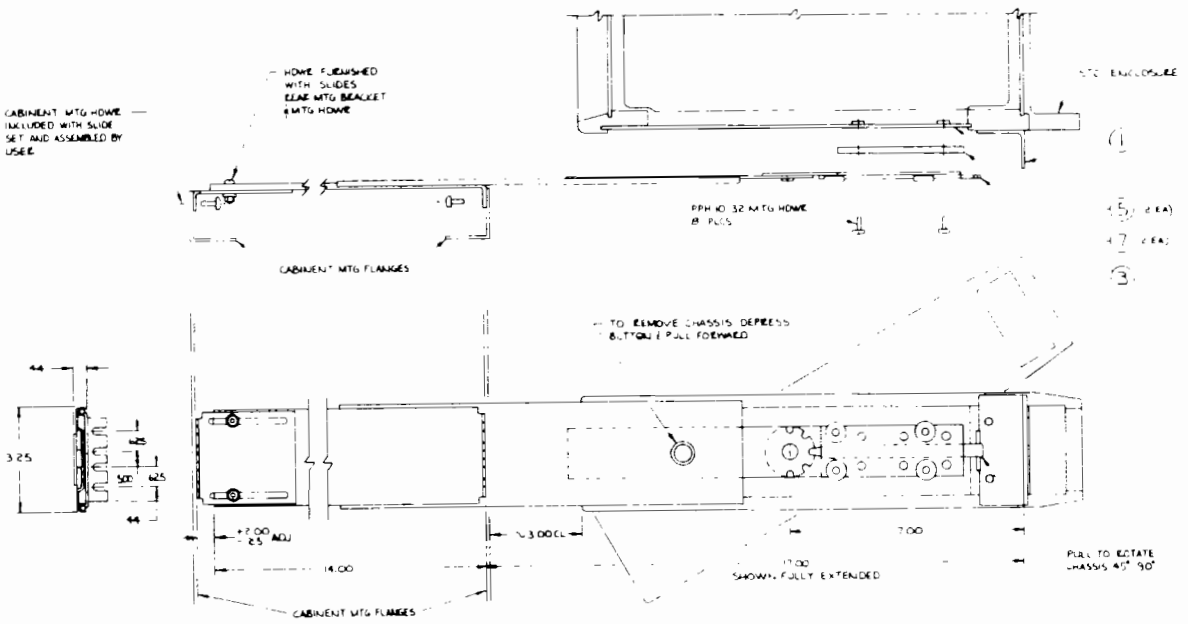
OPTION 10
CHASSIS SLIDE

Option 10 equips your counter with the hardware required to mount the unit in a standard 19" wide console. With the chassis slide installed the counter can be serviced without removing it from the rack.

The option consists of:

OPTION 10 – 2010147

①	Rack Mount Kit	– 2010008-01
③	Slide Set	– 5000189
⑤	Side Panels	– 5210179
⑦	Spacers	– 5210249



1. All MTG HDWR and hole spacing conforms to MIL-STD-189.
2. To install slides in field; Remove top cover and top frame; Mount special side panels (5210179) on Std. enclosure.
3. Item numbers within ○ symbol are on P/L 2010147. All other items assembled or exploded are shown for clarification or reference only.

Figure 010-1. Side View of Counter with Option 10 Installed

OPTION 12
INCREASED SENSITIVITY

Option 12 provides increased sensitivity by 5 dB guaranteed from 10 MHz to 18/26.5 GHz. The sensitivity specifications with Option 12 are:

10 MHz	– 1 GHz	-20 dBm
1 GHz	– 12.4 GHz	-30 dBm
12.4 GHz	– 20 GHz	-25 dBm
20 GHz	– 26.5 GHz	-20 dBm

OPTION 13
MATE-CIIL INTERFACE

INTRODUCTION

This document defines the MATE-CIIL interface for the EIP Microwave Model 535B/538B Counter. It explains the general format and processing of CIIL operation codes, and gives a detailed definition of the CIIL operation codes used for the 535B/538B counter.

CIIL DESCRIPTION

CIIL stands for Control Interface Intermediate Language. It is a common interface language that operates with associated protocols between a computer subsystem and instrumentation connected to it via an IEEE 488 communication bus. The environment is expected to be an automatic test station. It is the intent of this interface to allow for the interchangeability of IEEE 488 compatible instrumentation with minimum impact upon other system elements.

The GPIB interface of the 535B/538B counters is fully compatible with the IEEE 488-1978 standard. With the GPIB interface, the counter can respond to remote control instructions and can output measurement results via the IEEE 488-1978 bus interface.

FUNCTIONAL SUMMARY

This interface provides the following functions:

* Accepts control computer input and translates the standard program instructions of the MATE-CIIL into those required by the 535B/538B counter.
* Establishes the timing required to operate in the MATE Test Executive environment.
* Formats measurement responses and transmits upon request to the control computer.
* Provides the means to perform confidence and built-in tests.
* Controls input signals.
* Generates status messages.

GENERAL RULES FOR INPUT AND OUTPUT

INPUT

CIIL input commands implemented in the EIP 535 and 538 Counter are shown in Table 1 below.

TABLE 1

COMMAND	DESCRIPTION
<verbs>:	
FNC	function
INX	initiate
FTH	fetch
OPN	open
CLS	close
STA	status
RST	reset
CNF	confidence test
IST	built in test
GAL	go to alternate language
<set codes>:	
SET	set
SRX	set maximum
SRN	set minimum
<nouns>:	
ACS	AC signal
RPS	ramp signal
TRI	triangular wave signal
SQW	square wave
WAV	waveform
<chan num>:	
:CH1 or :CH01	band 1
:CH2 or :CH02	band 2
:CH3 or :CH03	band 3
<modifiers>:	
VRMS	voltage-TRMS
FREQ	frequency
FRES	frequency resolution
TIMP	test-equip-IMP

FORMAT OF INPUTS

There are nine transmission commands applicable to the counter in the CIIL language. At the start of each command, the instrument is listen-addressed by the control computer. The end of transmission is indicated by <cr, lf>. Each transmission command begins with its own characteristic <verb>. They are as follows:

FNC	(function) set up the instrument
INX	initiate a measurement
FTH	(fetch) transmit results to the control computer
CLS	close the primary input path
OPN	open the primary input path
RST	reset the instrument
STA	report status
IST	initiate built-in test
CNF	initiate confidence test
*GAL	go to alternate language

* NOTE:

Once the controller issues the GAL string, the counter goes to native language mode. The way to return to MATE-CIIL mode is by issuing MA string, DCL or power on (see paragraph 3.12).

GENERAL RULES

It takes a specific amount of time for the counter to process the input data (error checking, formatting, changing the mode of operation, etc.). To prevent the data rate of the bus from slowing down while the counter is doing input data processing, the data is accepted as soon as it is available on the bus, and it is temporarily stored in memory. The size of the storage memory is 148 characters. This is the maximum length of any one command string.

All strings are processed and requested actions performed independently. No string depends on a previous string or setup except as specified. There are no incremental or partial setups. If the FNC string is not complete, or contains an error, the counter does not use information from the last setup to complete or correct the current one. Rather, an error message is generated for transmission to the control computer and the counter reverts to the state that it was in just before the error message was processed.

Anywhere one blank, <b>, is indicated, the instrument accepts multiple blanks as if they were one blank.

The following notation describes the various input (and output) strings.

|	= exclusive OR
<b>	= one ASCII blank
[ ]	= optional field
. . .	= field that may be repeated as often as required
<set code>	= SET | SRX | SRN
<noun>	= three ASCII characters (see Table 1)
<modifier>	= four ASCII characters (see Table 1)
<mchar>	= FREQ
<chan num>	= 1 | 2 | 3 | 01 | 02 | 03
<value>	= any ASCII encoded number in floating point or integer or engineering notation. The maximum number of digits in the numeric integer without leading zeros is 12. The maximum number of digits in the exponent is 3 (with or without leading zeros).
<cr, lf>	=ASCII encoded carriage return and line feed.

OUTPUT

FORMAT OF OUTPUTS

After the transmission of the INX, FTH, and STA type strings, the counter responds with one of the following messages depending on which of the above three <verbs> was most recently received.

1. F07CTR1:<ASCII message><cr, lf>
2. F05CTR1:<ASCII message><cr, lf>
3. <b><cr, lf>
4. <b><value>

GENERAL RULES

After receiving the INX, FTH, and STA strings, the counter can be talk-addressed. It takes a specific amount of time for the counter to process the input string. If the controller talk-addresses the counter before the counter finished processing the input string, erroneous output may result. To prevent such erroneous output, the programmer must provide sufficient programmed delays or use the counter's Service Request status byte.

FORMAT AND PROCESS OF MATE-CIIL STRINGS

FNC STRING

FORMAT OF FNC

The information contained in FNC string for measurement setup must be encoded as follows:

FNC<b><noun><b><mchar><b>:CH<chan num>[<b><set code><b>
<modifier><b><value>]. . .<cr, lf>

As can be seen from the above, each optional field consists of :

<b><set code><b><modifier><b><value>

The order within the FNC string of each optional field is random and depends only on the programmer. The <mchar> field just after the <noun> indicates the parameter to be measured. As can be noted, the EIP 535/538 counter can measure frequency only.

<chan num> and <mchar> Relationship

The acceptable value of <chan num> depends on <mchar>. <chan num> meanings and allowable combinations are shown below:

<chan num>	counter band	<mchar>
1 or 01	1	FREQ
2 or 02	2	FREQ
3 or 03	3	FREQ

If any other <chan num>/<mchar> combination appears in the FNC string, an error message will be generated for transmission to the control computer.

<chan num>, <noun>, and <modifier> RELATIONSHIP

CHANNEL NUMBER	VALID NOUN	VALID MODIFIER	MEASURED CHARACTERISTIC
1	ACS TRI RPS SQW WAV	VRMS FREQ TIMP FRES	10 Hz $\leq$ frequency $\leq$ 100 MHz
2	See above	See above	10 Hz $\leq$ frequency $\leq$ 1 GHz
3	See above	See above	0.95 GHz $\leq$ frequency $\leq$ 26.5 GHz (Note 1, 2)

NOTE 1: For 535 the value is 18.5 GHz
NOTE 2: For 535 the value is 20 GHz if Option 11 is included
NOTE 3: For 538 the value is 26.5 GHz

PROPERTIES OF <set code>

All <modifiers> for the counter may appear as many as 3 times, each with a different <set code> and <value>. However, only one <value> will be used. The correct one shall be determined by the following priority lists:

SRX
SET
SRN

This means that if SRX is missing, then the <value> associated with SET is used. If SET is also missing, then the <value> associated with SRN is used.

MEASUREMENT SETUP

The counter is capable of only one measurement. Therefore <mchar> can be only:

FREQ

If any other <mchar> is given, an error message will be generated for transmission to the control computer.

The only <modifier> which can have an effect on the counter setup is:

FRES

FREQUENCY RESOLUTION

The <value> associated with FRES will be rounded to the closest integer:

1	1E5
10	1E6
100	1E7
1E3	1E8
1E4	1E9

RANGE CHECKING

There are no necessary <modifiers> for the counter to make a measurement. The entire instrument setup can be determined by the FNC string (See 3.1). However, there are some <modifiers> which, if received, will cause the counter to do range checking.

The following <modifiers>, if present, are range checked as indicated as a function of <chan num>:

<chan num>	<modifier>	<value> range
1	FREQ	10 to 100E6
	VRMS	25E-3 to 120
	TIMP	1E6 only
2	FREQ	10E6 to 1E9
	TIMP	50 only
	VRMS	ignored
3	FREQ	.95E9 to 26.5E9 (Note 1,2)
	POWR	-30 to 7
	TIMP	50 only
	VRMS	ignored

Note 1: For 535 the value is 18.5E9.
Note 2: For 535 the value is 20E9 if option 11 is included.

FRES need not be range checked. If any <modifier> <value> is found to be out of range, an error message is generated for transmission to the control computer.

CLS STRING

FORMAT OF CLS

The counter connects to the outside world via three main input ports. A programmer who wishes to connect the instrument to one of these input ports issues the CLS command. This appears as a small string with only a <chan num> option:

CLS<b>:CH<chan num><cr, lf>

As with the FNC string, <chan num> depends on the input band the programmer wishes to use.

It is possible for the FNC, or setup string, to contain a <chan num> that is not the same as the one included in the CLS string. Although this would cause a measurement to be taken using a path that has not yet been closed, it is an acceptable setup since the actions of each transmission are determined independently (without knowledge of previous transmissions) except where indicated.

PROCESS OF CLS

The processing of CLS is the same as selecting the band on the counter. While processing the CLS command, the counter switches the Count Chain from a previously selected band to the one corresponding to a new input channel number.

OPN STRING

FORMAT OF OPN

A programmer who wishes to disconnect the instrument from the input port issues an OPN command. This also appears as a small string with only a <chan num> option:

OPN<b>:CH<chan num><cr, lf>

PROCESS OF OPN

The OPN command implies that the instrument has the capability to logically isolate its input from the outside world via an internal mechanism controlled by the instrument itself.

When the channel specified in the OPN command is already open, the counter does nothing.

RST STRING

FORMAT OF RST

The format of the RST string is as follows:

RST<b><noun><b><mchar><b>:CH<chan nun><cr.lf>

All fields following the <verb> RST are ignored by the counter.

PROCESS OF RST

Upon receiving and processing this command, the counter performs a reset action that causes the following initialization configuration:

CLEAR DISPLAY
DISPLAY ACTIVE
SELECT BAND 3
RESOLUTION 3
FAST PASSIVE
HOLD PASSIVE
OUTPUT TO DISPLAY AND GPIB

CNF STRING

FORMAT OF CNF

The confidence test operation code CNF has the following format:

CNF<cr, lf>

It is not part of the run-time scenario. After this message has been transmitted, the control computer must wait a specified amount of time, depending upon the resolution of the counter before continuing to communicate to the counter.

RESOLUTION	WAIT TIME
0	1 second
10	100 millisecond
100	10 millisecond
1000 or above	1 millisecond

Within this "CNF time," the counter completes the confidence test and should not be interrupted by any command. Commands sent during the CNF time may cause failure of the test. After the test is over, the counter accepts any command string. However, in general, the CNF string is followed by the STA string.

PROCESS OF CNF

The confidence test is an end-to-end test to determine whether the instrument is functioning properly. The process of CNF verifies that the Count Chain, Gate Generator, and the VCO are operational.

At the end of the test, the counter should show 200 MHz on the display. Otherwise an error message will be generated.

The test status can be accessed by the STA string.

IST STRING

FORMAT OF IST

The format for built-in test is as follows:

IST<cr, lf>

It is not part of the run-time scenario. After this message has been transmitted, the control computer must wait a specified amount of time, depending upon the resolution of the counter, before continuing to communicate to the counter.

RESOLUTION	WAIT TIME
0	1 second
10	0.1 second
100	10 millisecond
1000 or above	1 millisecond

Within this "IST time," the counter completes the confidence test and should not be interrupted by any command. Commands sent during the IST time may cause failure of the test. After the test is over, the counter accepts any command string. However, in general, the IST string is followed by the STA string.

PROCESS OF IST

The confidence test is an end-to-end test to determine whether the instrument is functioning properly. The process of IST verifies that the Count Chain, Gate Generator, and the VCO are operational.

At the end of the test, the counter should show 200 MHz on the display. Otherwise an error message will be generated. The test status can be accessed by STA string.

STA STRING

FORMAT OF STA

The format of this transmission is as follows:

STA<cr, lf>

This string requires a response to be sent from the counter to the control computer. There must be at least 300 ms wait time for the control computer before the counter can be talk-addressed. Typically, the string is sent after the completion of the built-in test or confidence test, but it can be sent at any time.

PROCESS OF STA

There are two valid response to this STA string:

1. F07PCT1:<ASCII message><cr, lf>
2. <b><cr, lf>

Reply 1 is sent if an error has been detected in the information received in the FNC string. Also, this format is used when any failure is detected as a result of CNF or IST.

Reply 2 is used when there is no error to report either as a result of run-time request of STA or STA request following CNF or IST.

INX STRING

FORMAT OF INX

The format of this transmission is as follows:

INX<b><mchar><cr, lf>

The <mchar> included in this string must match that included in the last previous FNC transmission. If it does not, an error message is generated for transmission to the control

computer. An error message is also generated if any one of the following strings are received just prior to the receipt of the INX transmission:

CNF
IST
RST
IEEE-488 bus command DCL

These would indicate that the instrument is being requested to initiate a measurement without information about to the measurement setup.

Once the INX transmission is sent by the control computer and its receipt acknowledged by the counter, the control computer then talk-addresses the counter. At this time the counter responds with either of the two transmissions:

1. <b><time><cr, lf>

   <time> := ASCII integer in seconds

2. F07PCT1:<ASCII message><cr, lf>

   (see paragraph 3.7.2)

Transmission 1 indicates that all previous FNC string and INX string information is valid and that the counter is prepared to make a measurement of the type requested by the most recent FNC string. <time> is a number indicating the instrument's calculated estimate of the time required to make the measurement and acquire the requested data. The method of this calculation is described in paragraph 3.8.2.

Transmission 2 indicates one of the following fault messages:

1. CIIL syntax error as described throughout this specification. The syntax error may have occurred in any string since the last talk address.
2. Any other error specified in the ERROR MESSAGE section of the 535/538 counter manual.

PROCESS OF INX

The sequence of events in response to the INX is as follows:

1. The instrument sends back <time> within 2 seconds of being talk-addressed.
2. The real-time clock of the counter begins to count an amount of time that equals:

   <c time> = <time> - 2 seconds

3. Once the clock has been started, the instrument begins to the required signal data.
4. If the counter is not able to make a reading in <c time>, an error message is generated for transmission to the control computer upon receiving and processing of the FTH string. The format of this error message is described in paragraph 3.7.2.
5. If the counter is able to make the measurement, the results are saved and transmitted to the control computer upon receipt and processing of the FTH string.

TIMING CALCULATION

As indicated in the previous paragraph, <time> is returned to the control computer when the counter is talk-addressed after accepting the INX transmission. The counter has 2 seconds to respond. <time> is calculated as follows:

<time> = <c time> + 2

<c time> is the time the counter allows for itself to capture the data, and prepare the data to be returned upon receipt of the FTH string. It is calculated as follows:

If the counter is in search mode:

<c time> = measurement time + acquisition time

If the counter is in measure mode:

<c time> = measurement time

The value of <time> ,needs to be only a rough estimate because it is used by the control computer just as a bus time-out for the talk-address following the FTH string. If the counter answers any time before <time> runs out in the control computer, the data is accepted, allowing the testing to proceed sooner.

FTH STRING

FORMAT OF FTH

The format of this transmission is as follows:

FTH<b><mchar><cr, lf>

The <mchar> included in this string must match that included in the last previous INX transmission. If it does not, an error message is generated for transmission to the control computer. An error message is also generated if the counter receives any one of the following strings just prior to the receipt of the FTH transmission:

CNF
IST
RST

These would indicate that the instrument is being requested to return an answer to the control computer without having taken a measurement.

Once the FTH transmission has been sent by the control computer and its receipt acknowledged by the counter, the control computer then talk-addresses the counter. At that time, the counter responds with any one of the following three transmissions:

1. <b><value><cr, lf>

2. F07PCT1:<ASCII message><cr, lf>

3. F05PCT1:<ASCII message><cr, lf>

Transmission 1 indicates that the information in all of the previous FNC strings, as well as any other strings, was valid. The measurement result is represented by <value>.

Transmission 2 indicates the following fault message:

CIIL syntax error as described throughout this specification. The syntax error may have occurred in any string since the counter was last talk-addressed.

Transmission 3 indicates the following fault message:

The measurement "timed out"; in other words, the counter was not able to detect a signal and make a measurement in the time it specified in response to the INX string.

PROCESS OF FTH

The measurement data captured as a result of receiving and processing the INX string is formatted upon receipt and acknowledgment of the FTH string. The format is as follows:

<b><value><cr, lf>

There are no blanks anywhere in the <value>. The only allowable ASCII characters are:

0 1 2 3 4 5 6 7 8 9 + - . E

The FTH string is roughly equivalent to the following counter command:

CIIL STRING	COUNTER EQUIVALENT
FTH FREQ	output frequency

GAL STRING

FORMAT OF GAL

The format of this string is:

GAL<cr, lf>

This <verb> is used to indicate that the next ASCII transmission is in the native language of the counter. Any command defined in the GPIB section of 535/538 counter manual may be used as long as it is in its native mode.

MA STRING

The way to return to MATE-CIIL mode is by issuing the string:

MA<cr, lf>

The IEEE-488 bus command DCL can not cause the counter to switch back to MATE-CIIL mode.

NOTE:

After transmitting the MA string, the controller must wait until the counter finishes processing the MA string before sending any other string to the counter. In this circumstance, using the counter's Service Request byte is recommended.

ERROR MESSAGES

The following error messages are added as a MATE option of 53X counter. When an error occurs, an error number will be displayed on the front panel as well as output through GPIB when the counter is talk-addressed.

The GPIB output format for error 95 is:

F05PCT1: NO SIGNAL FOUND

For others:

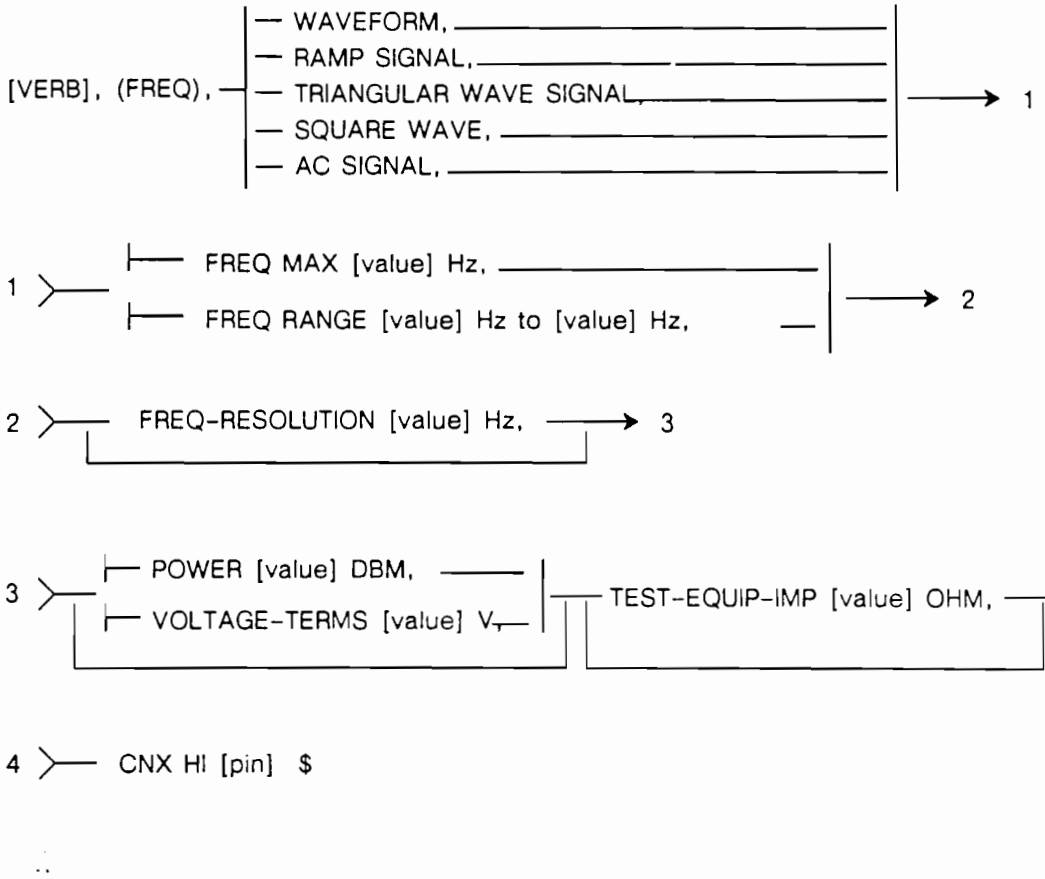
F07PCT1: ERROR NUMBER # (error number)

Detailed description of other error messages:

08	BIT test fail (200-MHz self test fail)
52	illegal power entry
53	illegal VRMS entry
54	illegal TIMP entry
55	illegal FREQ entry
75	undefined CIIL verb
76	undefined CIIL noun
77	undefined CIIL mchar
78	undefined CIIL channel number
79	illegal CIIL set code
80	undefined CIIL modifier
81	illegal CIIL value entry
82	illegal CIIL input format
85	<mchar> does not match <mchar> defined in last setup
86	<mchar> does not match <mchar> defined in last initialization
87	initialize prior to instrument setup
88	illegal <noun>/<mchar> combination

CIIL SYNTAX DIAGRAM

FREQUENCY MEASUREMENT:



Appendix A
Accessories

590 CABLE KIT OPTION 91 REMOTE SENSOR

The service kit for the 535B/538B counter will contain the following items.

2000017 - SERVICE KIT
2020147 - GPIB/BCD EXTENDER CARD
2020184 - STANDARD EXTENDER BOARD
2020185 - BAND 2 EXTENDER BOARD
2020221 - CABLE, BNC TO SELECT
2040222 - CABLE, BNC TO PC JK
2610054 - TEST CABLE, BNC E/Z HK
5000094 - IC EXTRACTOR TOOL

This kit is useful as a carrying case.

MODEL 590 FREQUENCY EXTENSION CABLE KIT

The kit, part number 2000025 contains:

1 - LO Cable (long) - 2040217
1 - IF Cable (short) - 2040218
1 - Adaptor (SMA to TNC) - 2610063
0 - 5 - Remote Sensors (Options 91 thru 96)

	PART NUMBER	FREQUENCY RANGE
91	2030022-00	26.5 - 40 GHz

SPECIFICATIONS

BAND 4

Used with 538B/06 Counter and 590 Frequency Extension Kit

OPTION	91
SELECT BAND	41
Waveguide Band	Ka
Range	26.5-40 GHz
Sensitivity (typ)	-25dBm (-20 dBm min.)
Waveguide Size	WR-28
Waveguide Flange	UG-599/U
Max. Input (typ)	+5 dBm
Damage Level	+10 dBm
Aquisition Time	<1 sec

INSTALLATION

Before connecting the remote sensor to the frequency source, verify that the power level is within the limits specified for the sensor.

Connect the long LO cable from the upper jack to the remote sensor. When using the sensor option 91, use the SMA-TNC adapter in the 590 kit.

Connect the short IF cable from the lower jack to the Band 3 input.

CAUTION

Static discharge or ground loops can damage or destroy the diode in a remote sensor. ALWAYS connect the LO cable to the counter first, then touch the shield to the body of the sensor before connecting.

Be sure that the counter and waveguide port to which the sensor will connect have a common ground. If in doubt, connect with a ground strap before connecting the remote sensor.

OPERATION

After connection, select band 4 on the 538B counter (equipped with option 06). Select the band by:

Press 

NOTE

Frequency limits (low/high) only operates to 26.5 GHz.

REPAIR

If loss of sensitivity occurs, the diode may be damaged. the 91 sensor diode can be replaced.

To replace the 91 sensor diode, unscrew the knurled cap and pull out the diode. Replace it with a 1N53B type diode that can be ordered from the manufacturer.

Alpha Industries, Inc.
20 Sylvan Road
Woburn MA 01807

Or order from EIP by part number 27300053.

Appendix B
List of Manufacturers

FSCM	MANUFACTURER
0000X	Any Manufacturer of this product.
00656	Aerovox Inc., 740 Belleville Ave, New Bedford, MA 02741
00809	Croven Ltd., Whitby, Ontario, Canada
01121	Allen-Bradley Co., South Milwaukee, WI 53204
01295	Texas Instruments Inc., Dallas, TX 75222
02660	Amphenol Connector Div., Bunker Ramo Corp., Broadview, IL 60153
02735	Solid State Div. RCA Corp., Somerville, NJ 08876
04618	American Pamcor Inc., Paoli, PA 19301
04713	Motorola Inc., Semiconductor Div., Phoenix, AZ 85008
06665	Precision Monolithic Inc., 1500 Space Park Drive, Santa Clara, CA 95050
07263	Fairchild Semiconductor, Mountain View, CA 94040
08717	Sloan Company, Sun Valley, CA 91352
09353	C & K Components Inc., Watertown, MA 02172
11236	CTS of Berne Inc., Berne, IN 46711
11237	CTS, Keen, Paso Robles, CA 93446
12463	Optronics Mfg., 2420 S. 60th St., Omaha, NE 68106
14158	AVX, Filters, 10080 Willow Creek Rd., San Diego, CA 92131
14298	American Components Inc., Conshohocken, PA 19428
14433	ITT Semiconductor Div., West Palm Beach, FL 33401
14455	Quality Hardware Mfg. Co., 12605 Daphine, Hawthorn, CA 90250
14655	Cornell Dubilier, Dept. 150, Ave. L, Newark, NJ 07101
18324	Signetics Corp., Sunnyvale, CA 94086
23880	Stanford Applied Engineering Inc., Santa Clara, CA 95050
23036	Pamotor Inc., Burlingame, CA 94010
24546	Corning Glass Works, Bradford, PA 16701
26654	Varadyne Ind., Santa Monica, CA 90404
27014	National Semiconductor Corp., Santa Clara, CA 95051
28480	Hewlett-Packard Co., Palo Alto, CA 94304
29990	ATC Div., Phase Ind., Huntington Station, NY 11746
34257	EIP Microwave Inc., Santa Clara, CA 95134
34649	Intel Corp., 3585 SW 198th Ave., Aloha, OR 97005
51406	Murata Corp. of America, 1148 Franklin Rd., Marietta, GA 30068
56289	Sprague Electric Co., North Adams, MA 01247
59660	Tusonix Inc., 2155 Forbes Bldg., Tucson, AZ 85705
70903	Belden Corp., Chicago, IL 60644
71590	Centralab Div., Globe-Union Inc., Milwaukee, WI 53201
72136	Electro Motive Corp., Sub. of Int. Elect. Corp., Florence, Santa Clara, CA 95050
72259	Nytronics Inc., Pelham Manor, NY 10803
72982	Erie Technological Products Inc., Erie, PA 16512
73445	Amperex Electronic Corp., Hicksville, NY 11802
80031	Mepco/Electra Inc., Morristown, NJ 07960
80740	Beckman Instruments Inc., Fullerton, CA 92634
81349	Military Specification
86797	Rogan Bros. Inc., Skokie, IL 60076
91637	Dale Electronics Inc., Columbus, NE 68601
95275	Vitramon Inc., Bridgeport, CT 06601
98291	Sealectro, Mamaroneck, NY 10544
99800	Delavan Div. American Precision Industries, East Aurora, NY 14052

A110
FRONT PANEL
DISPLAY AND KEYBOARD
(2020140)

The Front Panel Display and Keyboard assembly (A110) is divided into two functional sections.

- Numeric display and annunciators
- Keyboard

NUMERIC DISPLAY AND ANNUNCIATORS

This section of the assembly contains 12 common anode seven-segment numeric display units (DS1-DS12). 2 green LEDs (DS37 and DS38), and a maximum of 24 yellow LEDs (DS13-DS36).

The 12 seven-segment LEDs are mounted side by side, with space between each third digit from the right. The corresponding cathode segments of the seven-segment LEDs are connected, and the drive signals come from segment drivers Q3 throught Q10. The signals to drive the digits come from the digit drivers located on the Front Panel Logic board (A111).

The 24 yellow LEDs (DS13-DS36) are divided into three groups of eight LEDs each. The anodes of all LEDs in each group are connected. The cathode of each LED in a group is connected to one of the segment drivers (Q3–Q10). With this arrangement each group of annunciator lights can be regarded as similar to one seven-segment LED. The digit drives for the three groups of annunciator lights also come from the Front Panel Logic board (A111).

The two green LED s (DS37 and DS38) are driven by Q1 and Q2. When these LED s light, they indicate that GATE and CONVERTER SEARCH are in operation.

KEYBOARD

This section of the assembly makes provision for a maximum of 25 (single-pole double-throw) switches, of which only are used. The switches are arranged in a 4 row by 6 column matrix, with the extra switch taking the row 4 column 7 position. The columns are connected to +5V through the resistor network (RN1) on the Front Panel Logic board (A111).

The keyboard is continuously scanned. The signals scanning the keyboard are derived from A111. To scan the keyboard, the 4 rows are grounded sequentially. When a row is grounded, and a key in that row is pushed, one of the columns will be grounded. This information is sent to the A111 board where key debouncing is performed.

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A110 FRONT PANEL DISPLAY AND KEYBOARD

2020140-02 C

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A110	Front Panel Display & Keyboard	2020140-01	1	EIP	34257
Q1 thru Q10	PNP, Amp.	4710019	10	MPS - D55	04713
R1	Comp, 4.7K, 5%, 1/4 W	4010472	2	RC07GF472J	81349
R2	Comp, 130, 5%, 1/4 W	4010131	2	RC07GF131J	81349
R3	R1				
R4	R2				
R5	Comp, 240, 5%, 1/4 W	4010241	8	RC07GF241J	81349
R6	Comp, 18, 5%, 1/4 W	4010180	8	RC07GF180J	81349
R7	R5				
R8	R6				
R9	R5				
R10	R6				
R11	R5				
R12	R6				
R13	R5				
R14	R6				
R15	R5				
R16	R6				
R17	R5				
R18	R6				
R19	R5				
R20	R6				
DS1 thru DS12	LED, Numeric, Indicator	2800024-01	12	TIL – 312	28480
DS13 thru DS36	LED, Lamp, Yel .15 X .25	2800020	24	MV53124	50522
DS37	LED, Lamp, Grn , .12 OD	2800018	2	MV5274	50522
DS38	DS37				
S1	Switch, Mon, SPDT	4500013	21	REK 71882	14433
S2 thru S5	Not Used				
S6 thru S25	S1				
	Spacer	5100084	1		
P1	9 pin Recept.	2620065	1	22 - 14 - 2094	0000A
P2	17 pin Recept.	2620067	1	22 - 14 - 2171	0000A
P3	13 pin Recept.	2620066	1	22 - 14 - 212	0000A

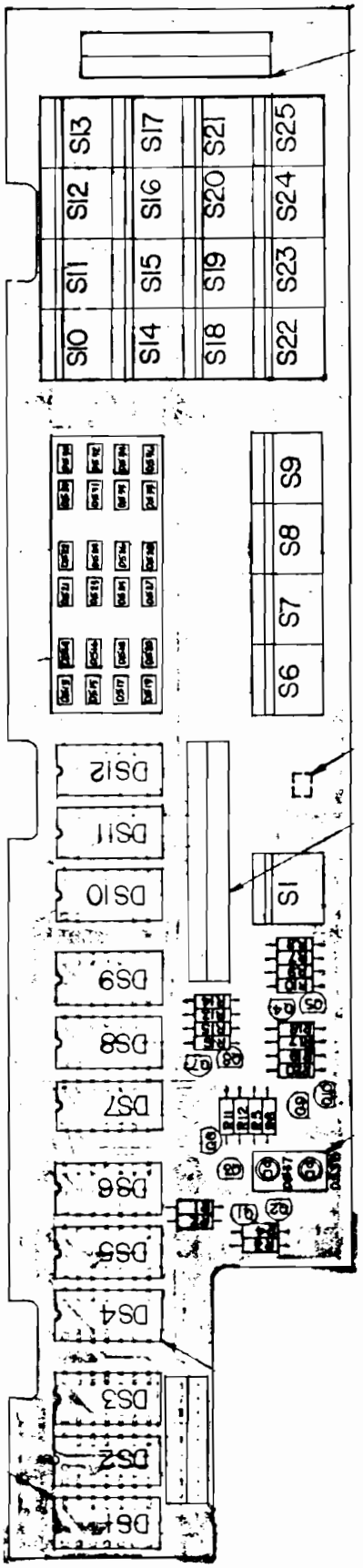
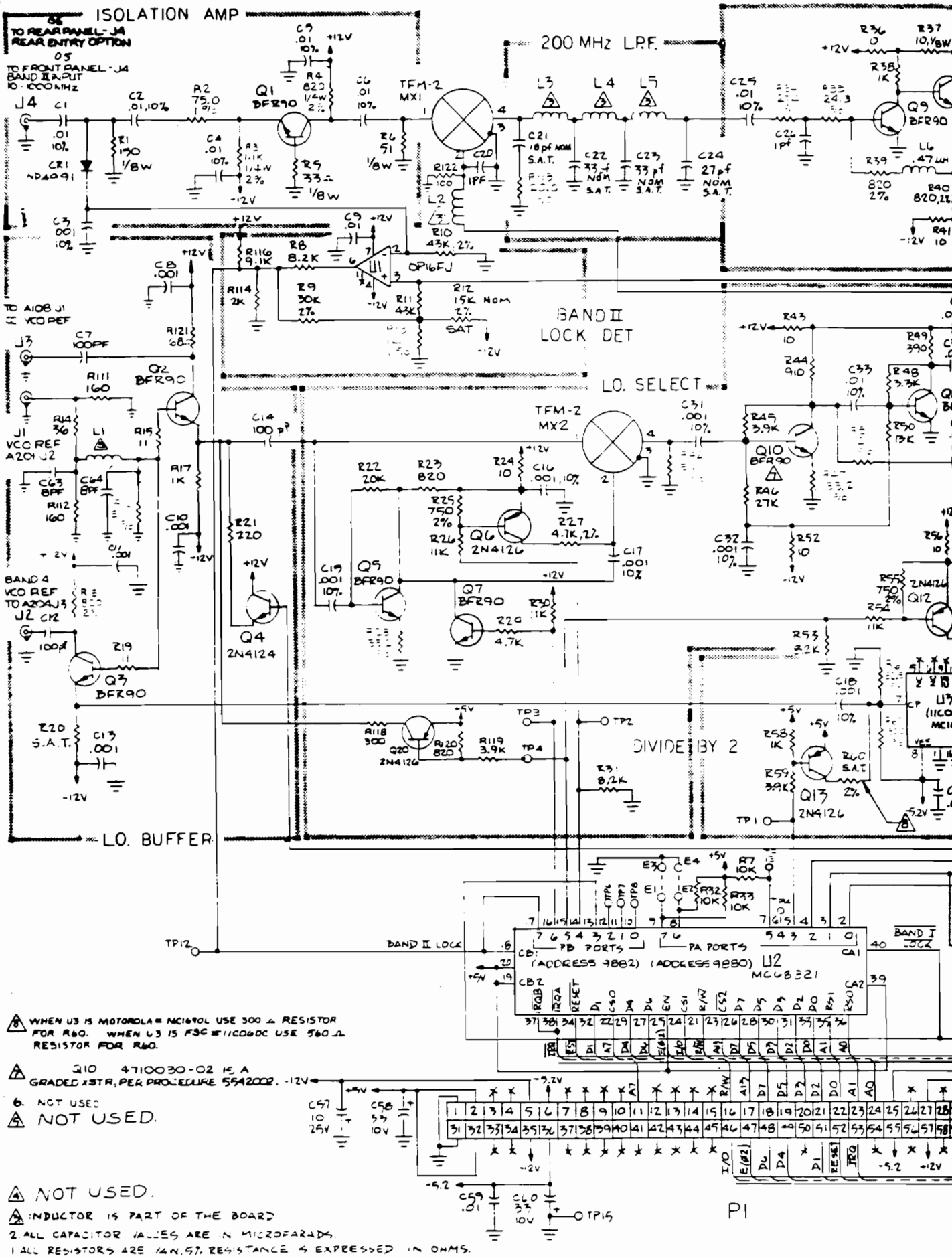
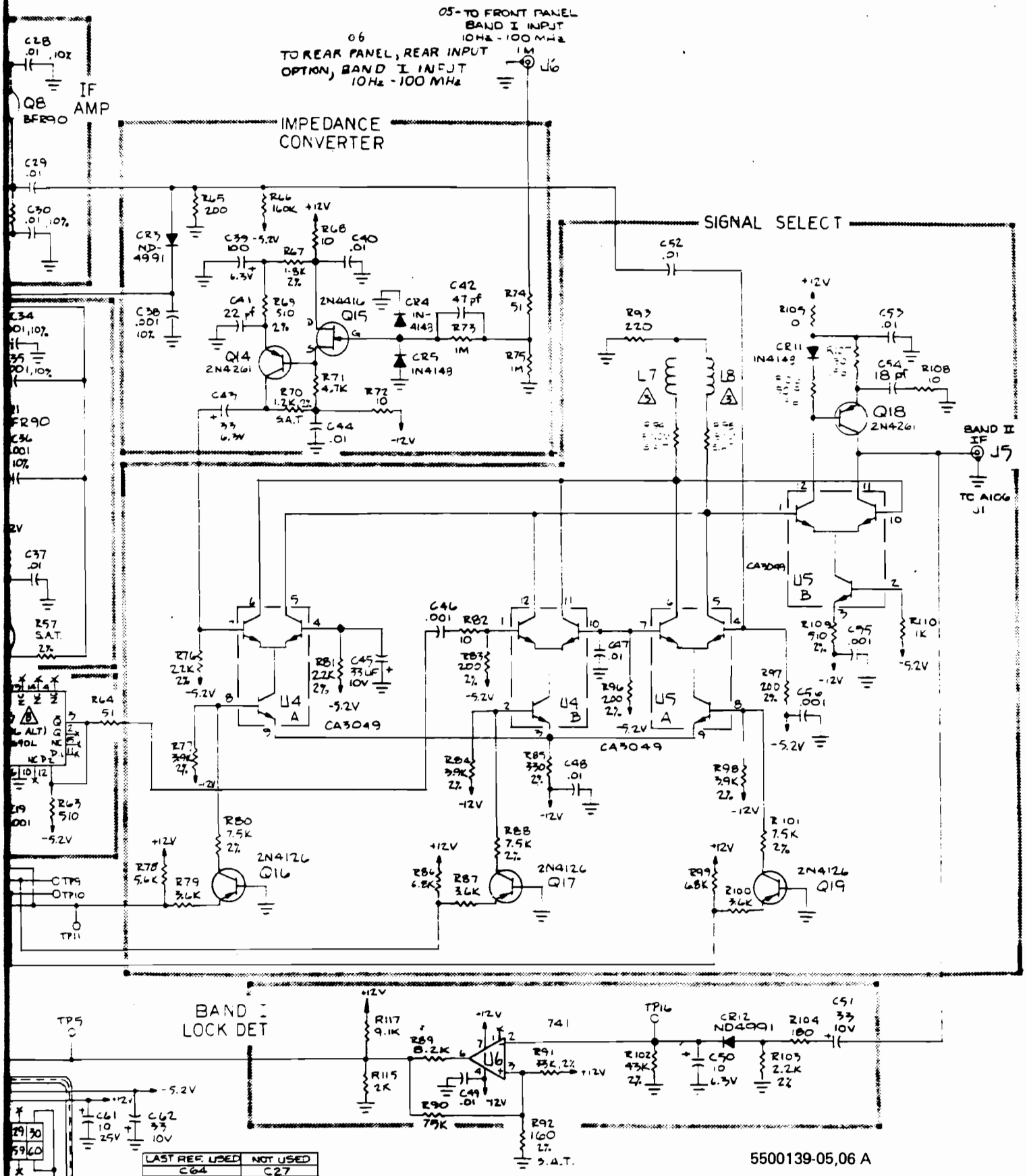


Figure 110-1. Front Panel Display and Keyboard Component Locator

5580034


ISOLATION AMP
TO REAR PANEL - J4 REAR ENTRY OPTION
TO FRONT PANEL - J4 BAND II INPUT 10 - 1000 MHz
200 MHz L.P.F.
TFM-2 MX1
TFM-2 MX2
BAND II LOCK DET
LO. SELECT
LO. BUFFER
DIVIDE BY 2
OP16FJ
TO A10B J1 = VCO REF
BAND 4 VCO REF TO A20A J3
J1 VCO REF A20A J2
BAND II LOCK
PB PORTS
PA PORTS
(ADDRESS 9882)
(ADDRESS 9880)
U2
MC6821
BAND I LOCK
P1
Q1 BFR90
Q2 BFR90
Q3 BFR90
Q4 2N4124
Q5 BFR90
Q6 2N4126
Q7 BFR90
Q9 BFR90
Q10 BFR90
Q12 2N4126
Q13 2N4126
Q20 2N4126
CR1 ND4091
L1
L2
L3
L4
L5
L6
SAT
S.A.T.
NOT USED.
NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTORS ARE 1/4W, 5% RESISTANCE IS EXPRESSED IN OHMS.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. INDUCTOR IS PART OF THE BOARD
4. NOT USED.
5. Q10 47100030-02 IS A GRADED XSTR; PER PROCEDURE 5542002. -12V
6. WHEN U3 IS MOTOROLA = MC1690L USE 300 Ω RESISTOR FOR R60. WHEN U3 IS FSC = 11C090C USE 560 Ω RESISTOR FOR R60.

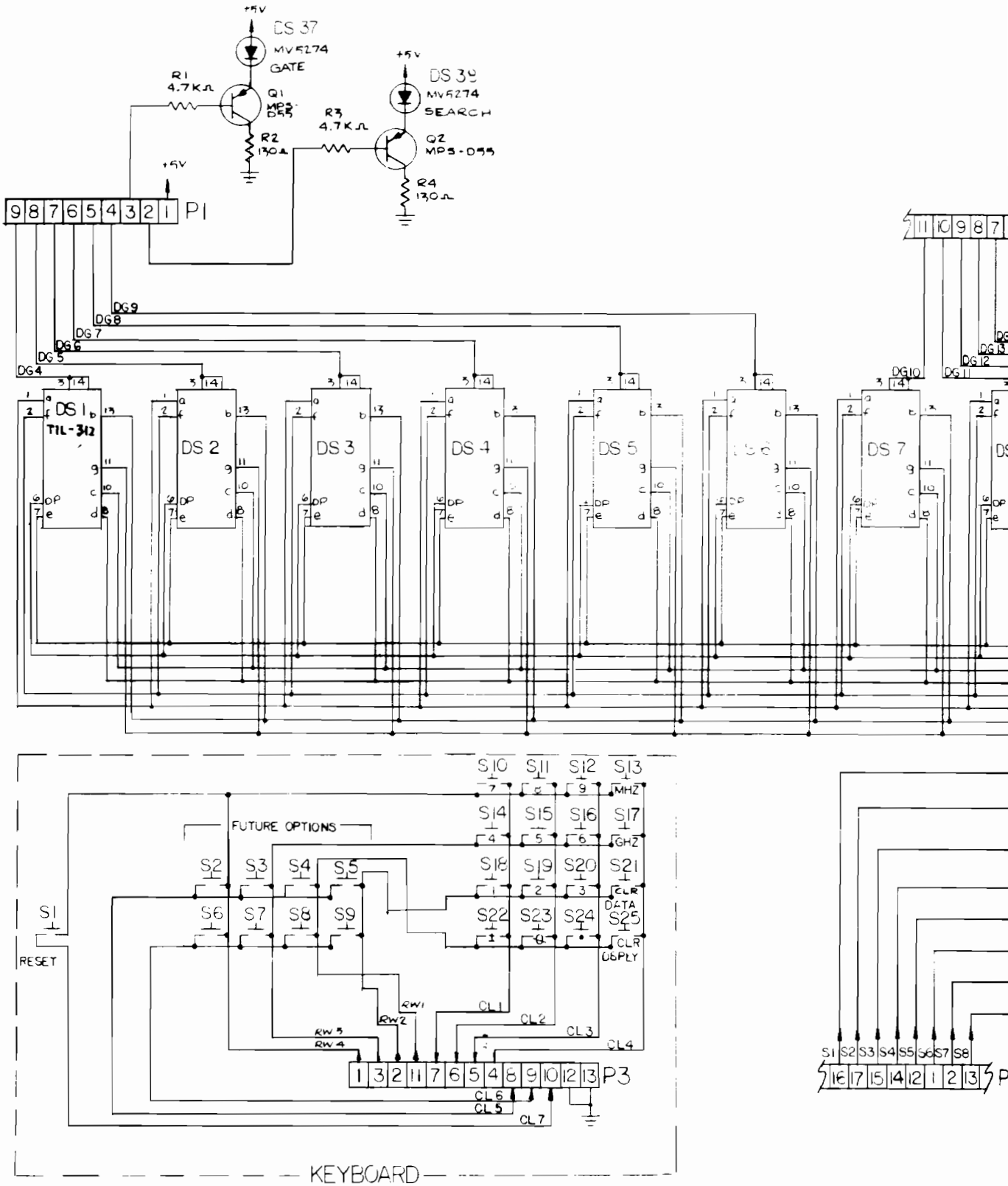


LAST REF. USED	NOT USED
C64	C27
CR12	E2,3,7,8,9,10
J6	
L8	
MX2	
Q20	
R122	
TP16	
U6	

5500139-05,06 A

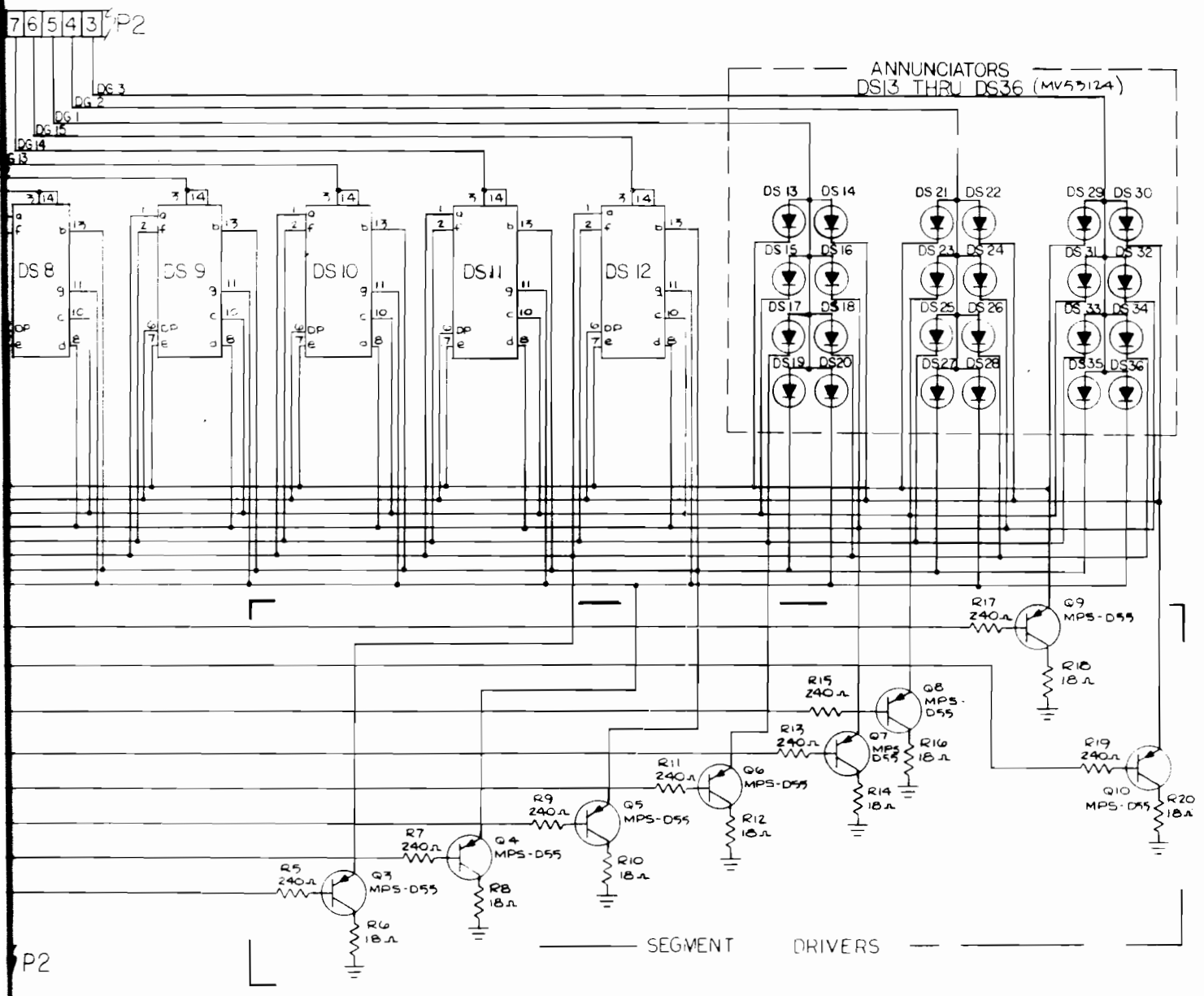
Figure 109-3. Band 2 Converter Schematic

5580034


+5V
DS 37
MV5274
GATE
R1
4.7KΩ
Q1
MPS-D55
R2
130Ω
R3
4.7KΩ
DS 39
MV5274
SEARCH
Q2
MPS-D55
R4
130Ω
9 8 7 6 5 4 3 2 1 P1
DG9
DG8
DG7
DG6
DG5
DG4
DG10
DG11
DG12
DG13
DS 1
TIL-312
DS 2
DS 3
DS 4
DS 5
DS 6
DS 7
S1
RESET
S2
S3
S4
S5
S6
S7
S8
S9
FUTURE OPTIONS
S10
S11
S12
S13
MHZ
S14
S15
S16
S17
GHZ
S18
S19
S20
S21
CLR
DATA
S22
S23
S24
S25
CLR
DSPLY
RW1
RW2
RW3
RW4
CL1
CL2
CL3
CL4
CL5
CL6
CL7
1 3 2 11 7 6 5 4 8 9 10 12 13 P3
S1 S2 S3 S4 S5 S6 S7 S8
16 17 15 14 12 1 2 13
KEYBOARD

ANNUNCIATORS

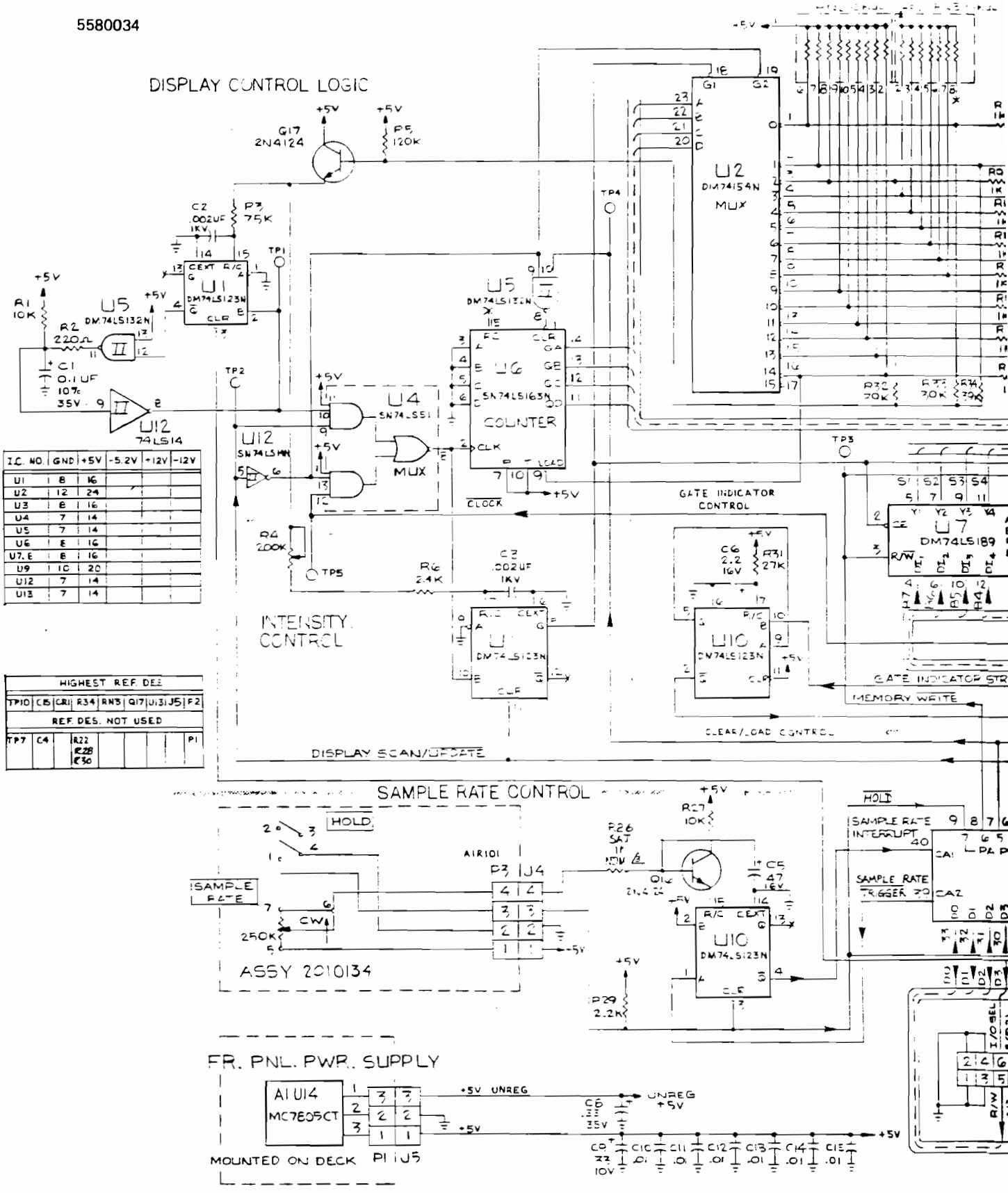
REMOTE		BAND
EXT. REF.		1 2
	OFFSET	3
	FRQ.	MLT



5500140-00 C

Figure 110-2. Front Panel Display and Keyboard Schematic

5580034



I.C. NO.	GND	+5V	-5.2V	+12V	-12V
U1	8	16			
U2	12	24			
U3	8	16			
U4	7	14			
U5	7	14			
U6	8	16			
U7, 8	8	16			
U9	10	20			
U12	7	14			
U13	7	14			

HIGHEST REF. DES.								
TP10	C15	CR11	R34	RN3	Q17	U13	J5	F2
REF. DES. NOT USED								
TP7	C4		R22 R28 R30					P1

3. SAT FREQUENCY RANGE 620 ~ MIN. - 1.2K MAX.
2. ALL CAPACITORS ARE EXPRESSED IN MICROFARADS. ALL .01 CAPS ARE 100V.
1. ALL RESISTORS ARE ¼W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED.

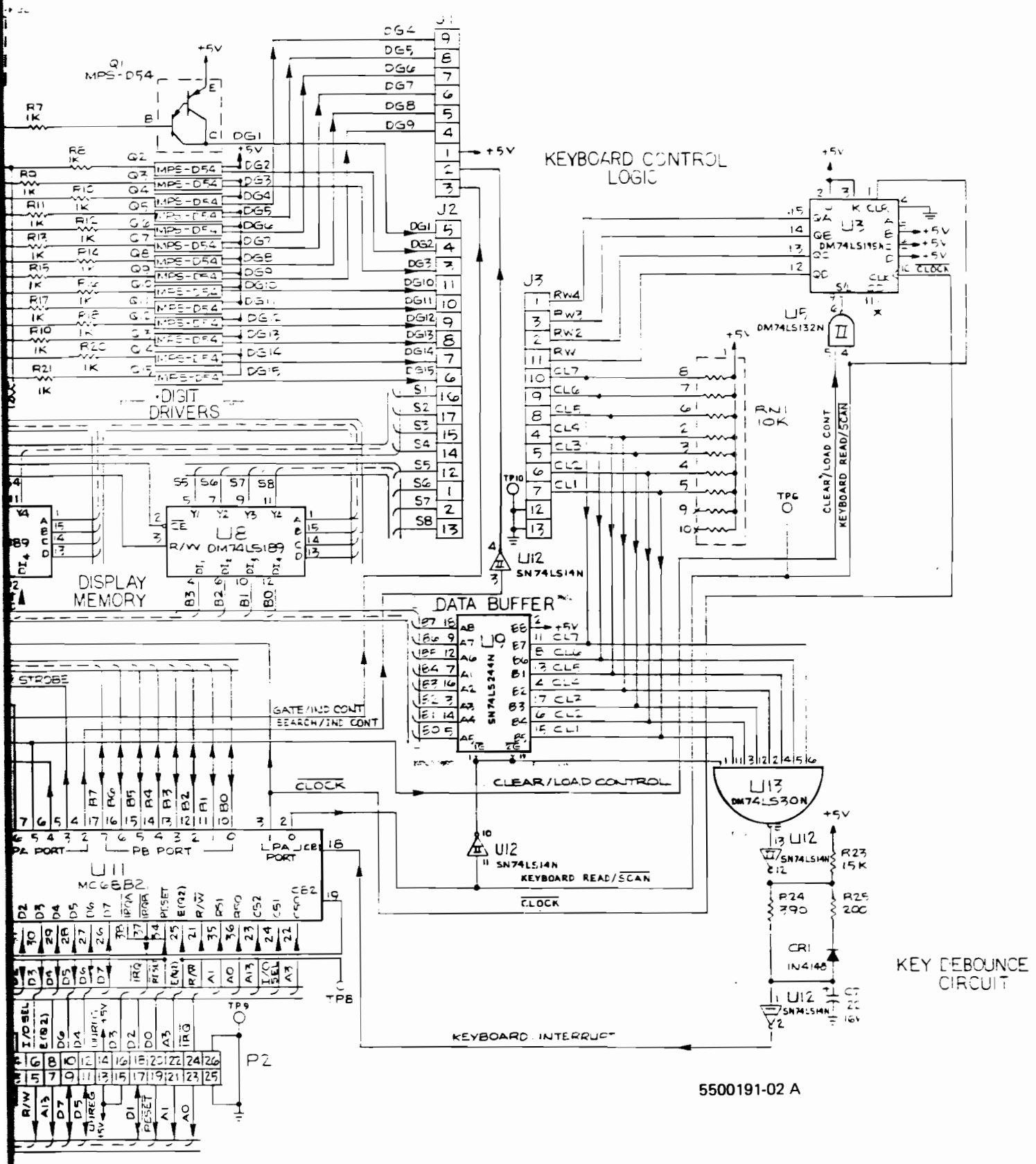
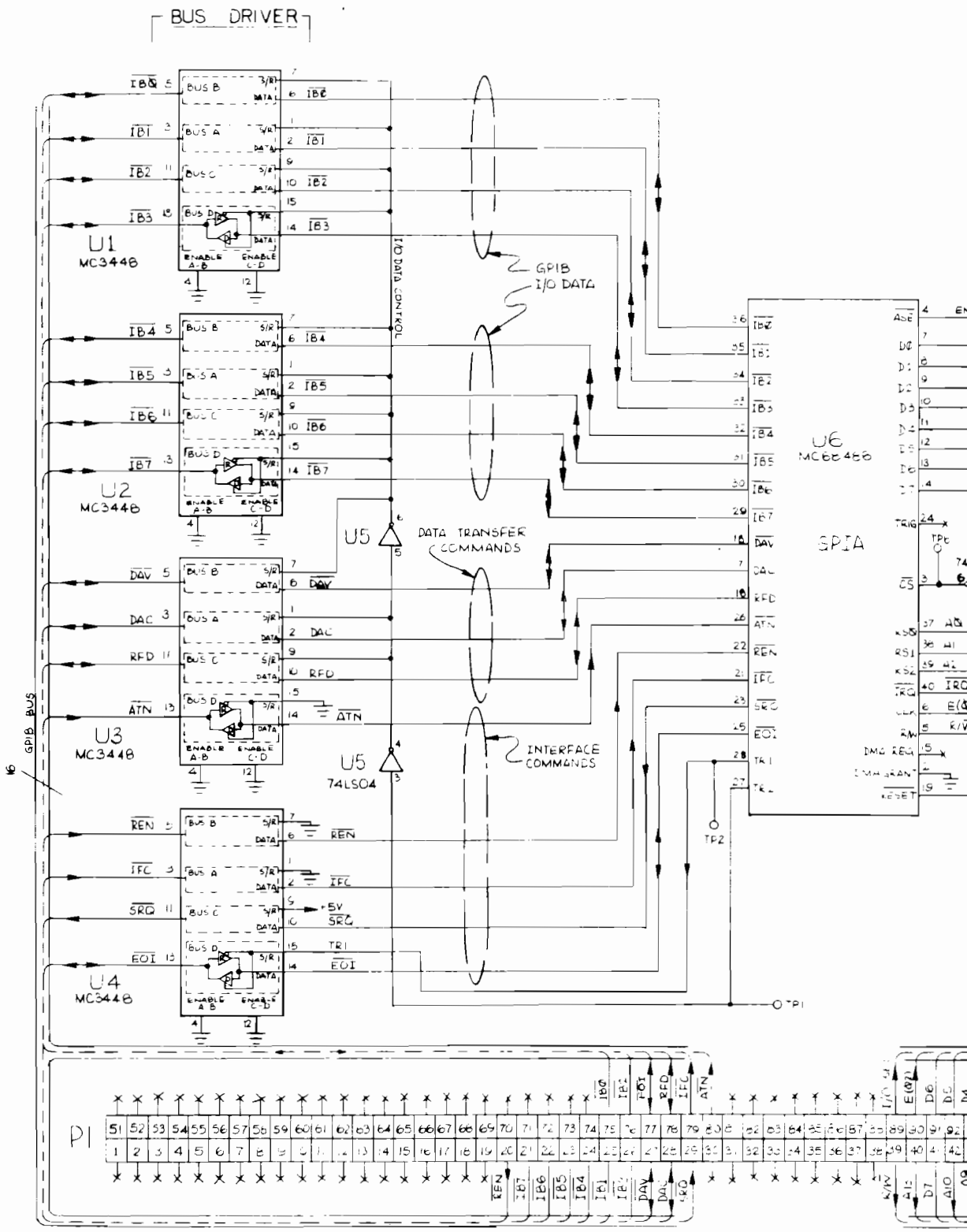
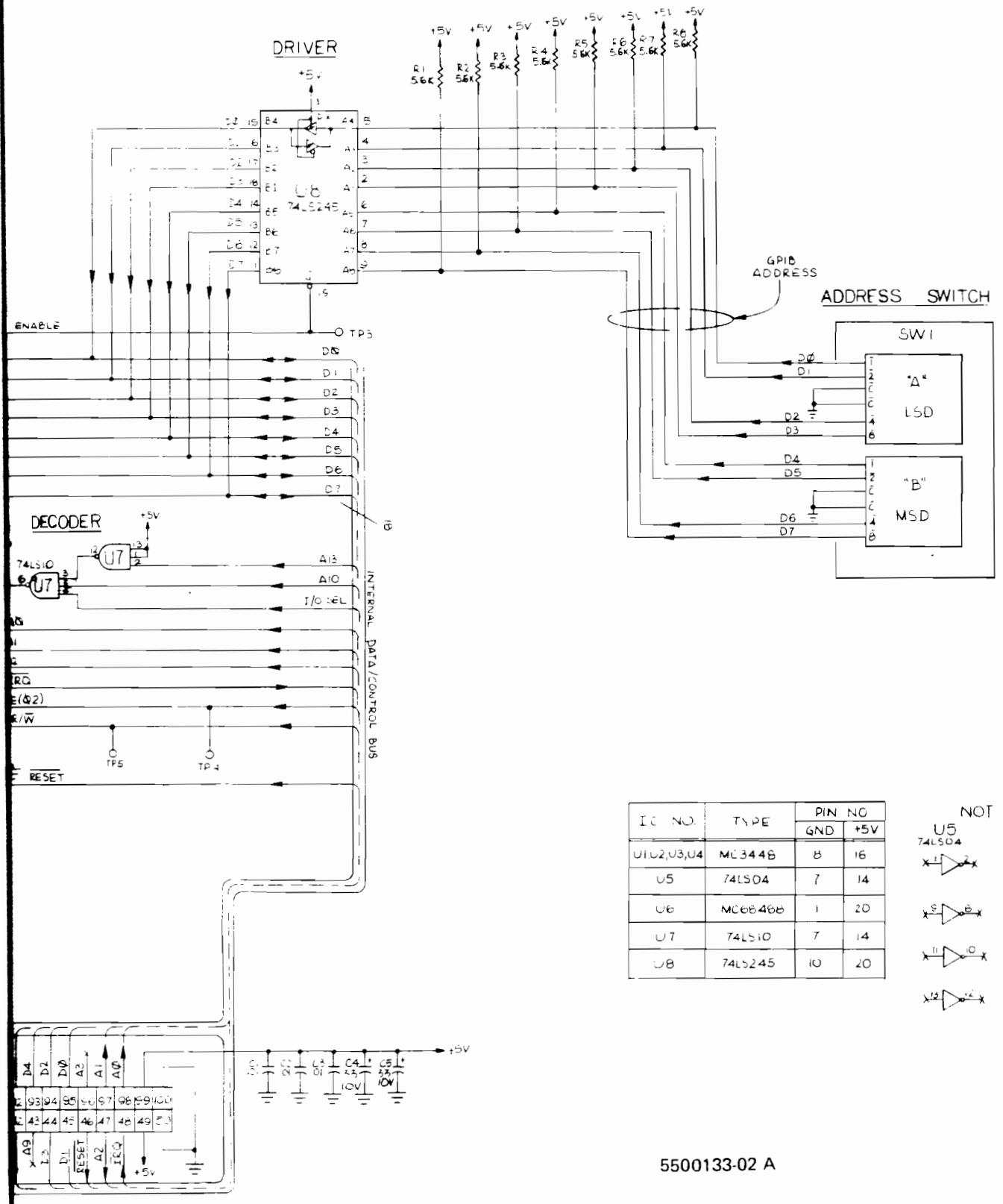


Figure 111-4. Front Panel Logic Schematic

5580034


BUS DRIVER
U1
MC3448
U2
MC3448
U3
MC3448
U4
MC3448
U5
74LS04
U6
MC68488
GPIA
GPIB BUS
I/O DATA CONTROL
GPIB I/O DATA
DATA TRANSFER COMMANDS
INTERFACE COMMANDS
TP1
TP2
P1



IC NO.	TYPE	PIN NO	
		GND	+5V
U1,U2,U3,U4	MC3448	8	16
U5	74LS04	7	14
U6	MC68488	1	20
U7	74LS10	7	14
U8	74LS245	10	20

NOT USED

U5 74LS04

U7 74LS10

5500133-02 A

Figure 08-4. GPIB Schematic

OPTION 09
REAR PANEL INPUT

Option 09 provides rear panel input for the 535B/538B counters by :

1. Reversing the converter assembly so that the Band 3 input connector protrudes through the hole in the rear panel that is identified as J113.

2. Reversing the Band 1 and Band 2 connectors to the holes marked J111 and J112 respectively on the rear panel.

NOTE: The specifications for the counter do not change when the input is from the rear panel.